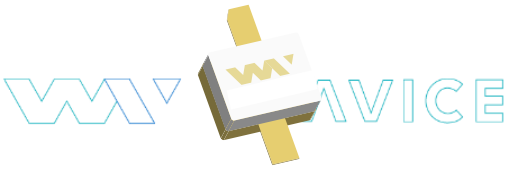
WVP60010F50A

DC – 6.0GHz 10W GaN Amplifier

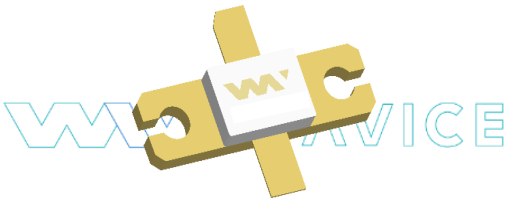
Features

- Frequency Range : DC – 6.0GHz
- Psat : 40.0 dBm
- Power Gain: 17dB @30dBm
- Small Signal Gain : 17dB
- DE: 45% @Psat
- Bias : V_D = 50V, I_{DQ} = 40mA, V_G = -2.5V (Typ.)
- Characterized at Pulse duty 10%, Pulse width 100uS

Product Image



- Package Type : SCN-BC1
- Package Dimensions: 5.1 x 8.13 x 1.57 mm



- Package Type : SCF-BC1
- Package Dimensions: 14.0 x 9.08 x 1.51 mm

Description

Wavice's WVP60010F50A is a high power, S-Band amplifier fabricated on Wavice's Durable 0.3um GaN on SiC process. Covering the frequency range of DC to 6.0GHz, the WVP60010F50A typically provides 40.0 dBm of saturated output power and 17 dB of power gain while achieving 45% Drain efficiency.
The WVP60010F50A is ideal for use in both commercial and military radar systems.

ROHS compliant.

Applications

- Military Radar
- Commercial Radar
- Infra Structure
- Small Cell

Ordering information

Part No.	Description
WVP60010F50A	SCF-BC1
WVP60010E50A	SCN-BC1
WVP60010F50AEV	WVP60010F50A Evaluation Board
WVP60010E50AEV	WVP60010E50A Evaluation Board

WVP60010F50A

DC – 6.0GHz 10W GaN Amplifier

Absolute Maximum Ratings

Parameter	Symbol	Value / Range
Drain Source Voltage	V_{DS}	55 V
Gate Source Voltage	V_{GS}	-10 to +2 V
Maximum Forward Gate Current	I_{GMAX}	1.2 mA
Absolute Maximum Channel Temperature	T_{CH}	+250 ℃
Storage Temperature	T_{STG}	-65 ℃ to +150 ℃
Mounting Temperature		245 ℃ / 30 sec

1) Case temperature T_C =25 ℃
2) Wavice does not recommend sustained operation above maximum operating conditions.
3) Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Symbol	Value / Range
Drain Source Voltage	V_{DS}	50 V
Drain Current	I_{DQ}	40 mA
Gate Source Voltage (Typical)	V_{GS}	-2.5 V
Case Operating Temperature		~40 ℃ to +85 ℃

1) Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.
2) Proper ESD(electrostatic discharge) control techniques should be used when handling these devices.

Thermal Characteristics

Parameter	Symbol	Units	Value	Test Conditions
Thermal Resistance using Infrared Measurement of Die Surface Temperature	R_{θ}(IR)	℃/W	13.15	Tbase = 85°C, V_D = 50V, I_{DQ} = 40mA, Freq = 3.7GHz
Peak IR Surface Temperature	T_{CH}	℃	102.5	

1) Thermal resistance determined to the case temperature (85 ℃)
2) Channel temperature indicated is an IR scan equivalent temperature, Thermal resistance is calculated using this value.

WVP60010F50A

DC – 6.0GHz 10W GaN Amplifier

Electrical Specifications

Parameter	Units	Min	Typ	Max
Saturated Output Power [1)]	dBm		40.0	
Drain Efficiency	%		50	
Power Gain @ 30dBm	dB		17	
Small Signal Gain	dB		19	
Input Return Loss	dB		-7	
ACLR	dBc		-38	
PAE	%		20	

Test conditions, unless otherwise noted :

- TA = 25 °C, V_D = 50V, I_{DQ} = 40mA, V_G = -2.5V(Typ.)
- Test Frequency : 3.7GHz
- Measured in WVP60010F50A Evaluation Board

1) Period 1msec / width 100usec, Duty 10%

Parameter	Units	Min	Typ	Max	Test Conditions
Gate Threshold Voltage	V	-3.8	-2.7	-2.0	V_{DS}= 10V, I_D= 1.2 mA
Drain-Source Breakdown Voltage	V	150			V_{GS}= -8V, I_D= 1.2 mA
Drain Current(I_{DMAX})[1)]	A	1.0	1.2		V_{DS}= 10V, V_{GS}= 2.0V
Gate Forward Voltage	V		2		I_{GS}= 1.2 mA

Test conditions, unless otherwise noted :

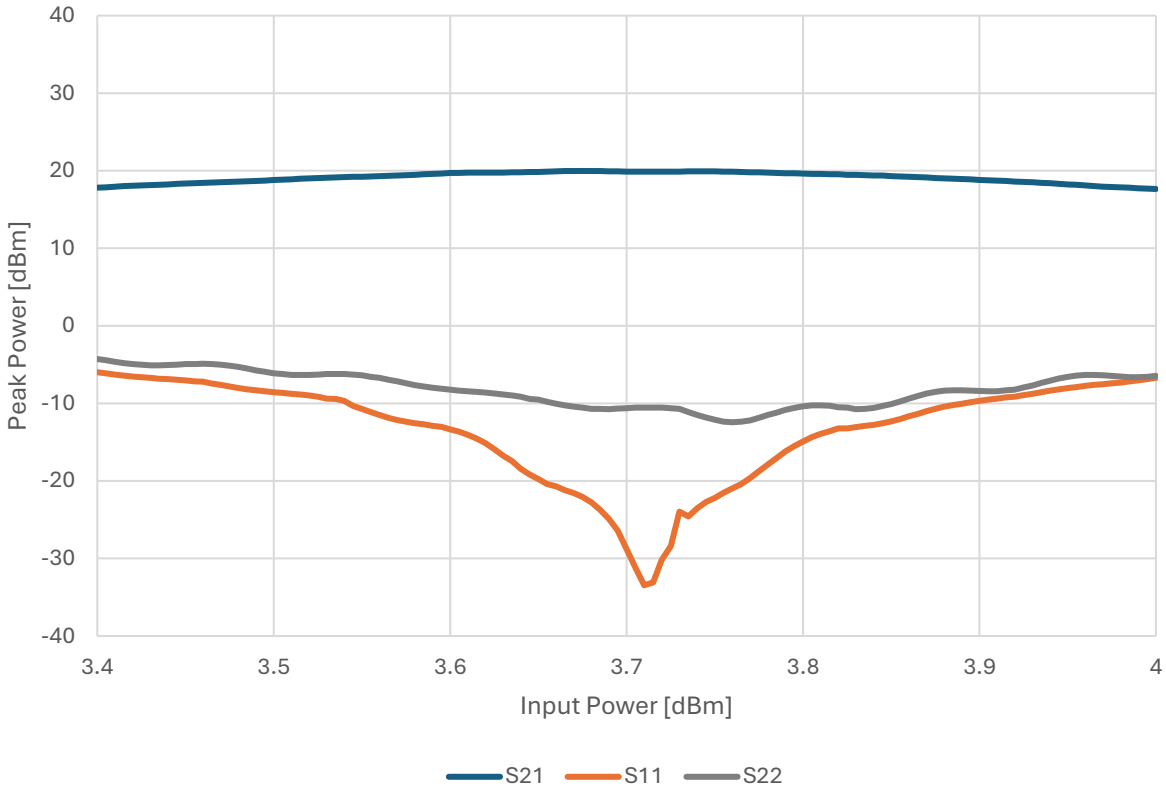
1) Scaled from PCM unit cell

WVP60010F50A

DC – 6.0GHz 10W GaN Amplifier

Performance Plots | S-Parameter

Test conditions, unless otherwise noted: T = +25 °C, V_D = 50 V, I_{DQ} = 40 mA

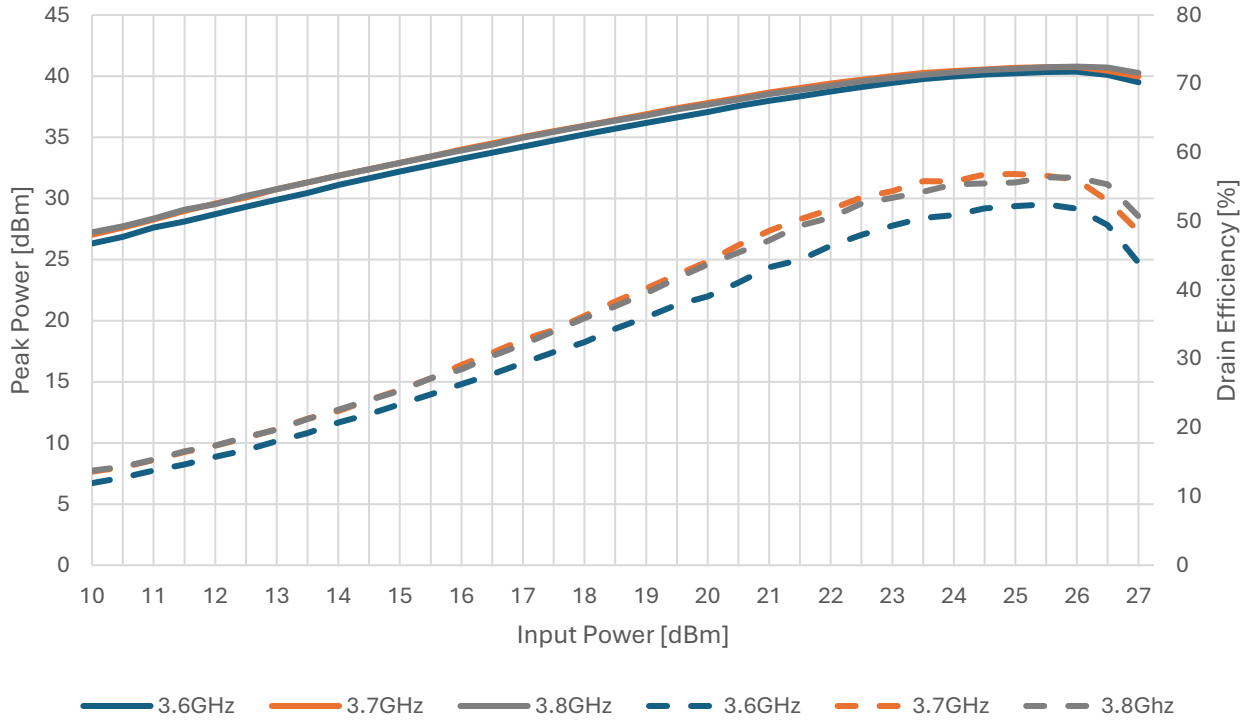


WVP60010F50A

DC – 6.0GHz 10W GaN Amplifier

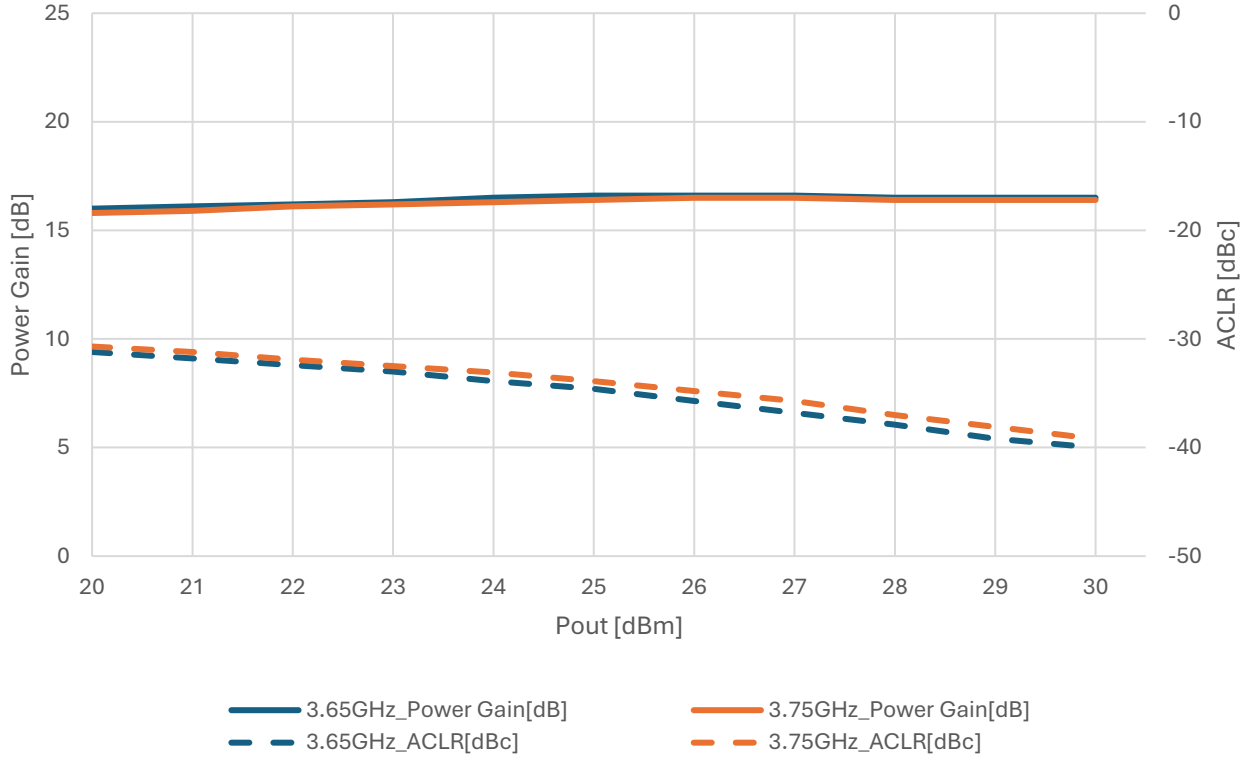
Performance Plots | Peak Power / DE vs Input Power

Test conditions, unless otherwise noted: T = +25 °C, V_D = 50 V, Pulse Width = 100usec, Duty Cycle = 10%



Performance Plots | Power Gain / ACLR vs Output Power

Test conditions, unless otherwise noted: T = +25 °C, V_D = 50 V, 5GNR 100MHz PAR 9.6dB



WVP60010F50A

DC – 6.0GHz 10W GaN Amplifier

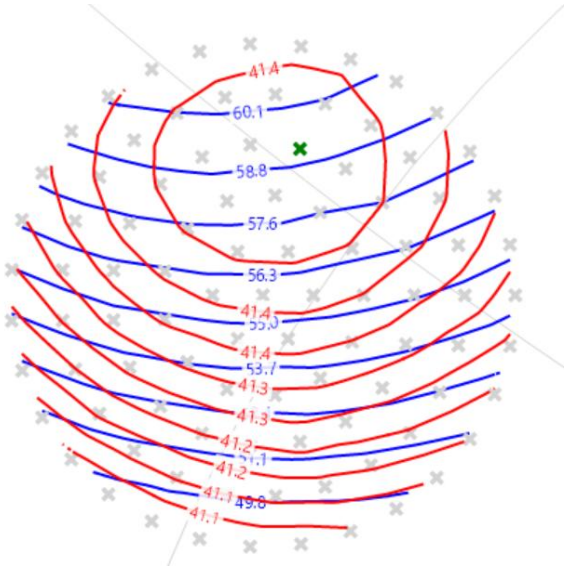
Load Pull Performance Plots | Power Matched

Test conditions, unless otherwise noted: T = +25 °C , V_D = 50V, I_{DQ} = 40mA, Pulse Width = 100usec, Duty Cycle = 5%

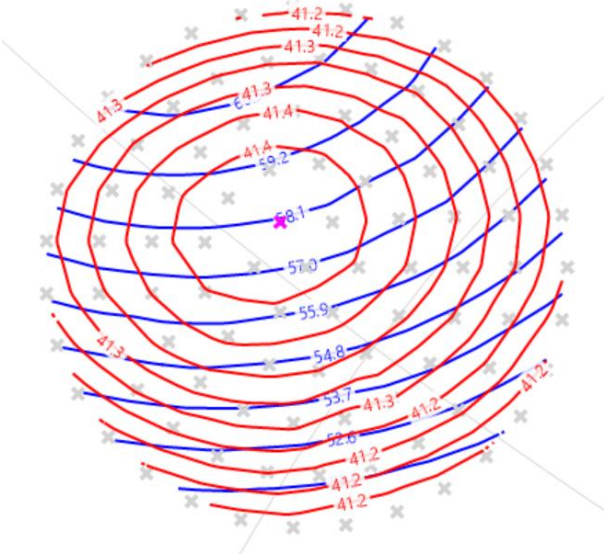
Freq (GHz)	ZL_F0	Zin_F0	Gain (dB)	Pout (dBm)	Pout (W)	Power Density (W/mm)	D.Eff(%)
3.6	22.61+25.50i	5.68-6.05i	15.92	41.48	14.07	11.73	59.23
3.7	21.52+25.92i	5.73-7.29i	15.66	41.40	13.83	11.52	58.04
3.8	20.31+25.59i	5.79+8.30i	15.58	41.35	13.65	11.37	59.37

Load Pull Contours | Power Matched

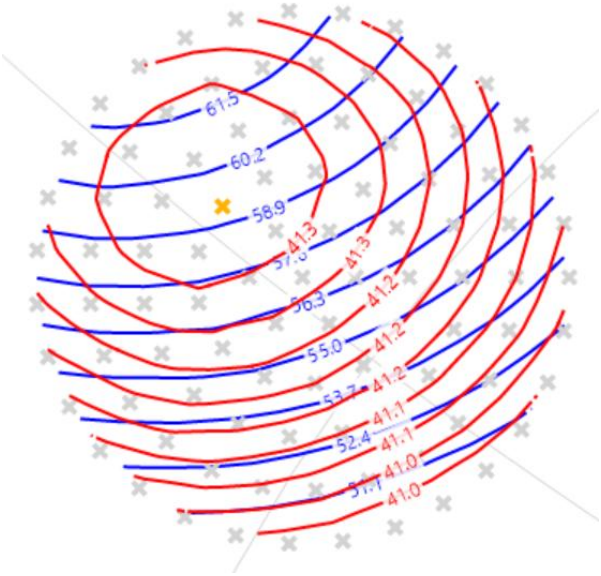
Test conditions, unless otherwise noted: T = +25 °C , V_D = 50V, I_{DQ} = 40mA, Pulse Width = 100usec, Duty Cycle = 5%



[3.6GHz]



[3.7GHz]



[3.8GHz]

WVP60010F50A

DC – 6.0GHz 10W GaN Amplifier

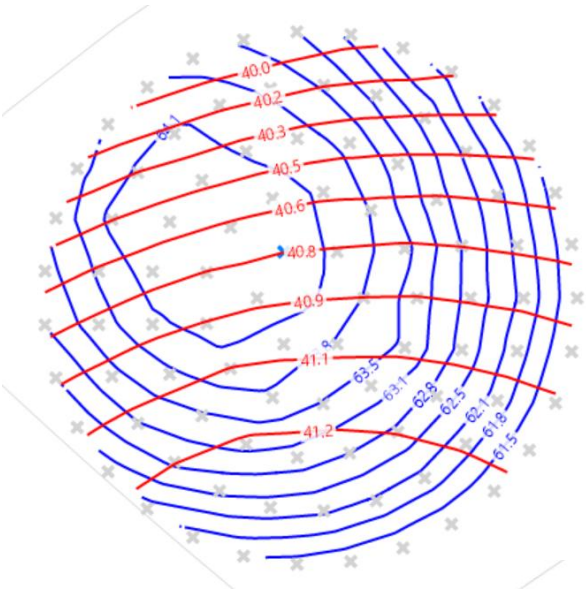
Load Pull Performance Plots | Efficiency Matched

Test conditions, unless otherwise noted: T = +25 °C , V_D = 50V, I_{DQ} = 40mA, Pulse Width = 100usec, Duty Cycle = 5%

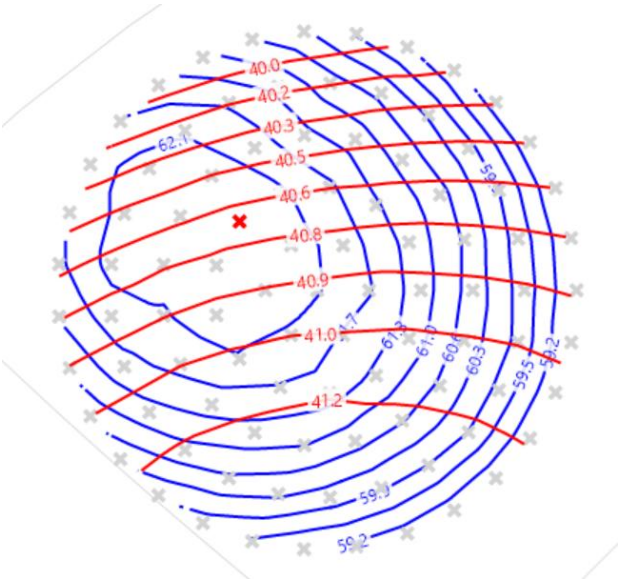
Freq (GHz)	ZL_F0	Zin_F0	Gain (dB)	Pout (dBm)	Pout (W)	Power Density (W/mm)	D.Eff(%)
3.6	15.09+30.43i	5.36+7.00i	15.41	40.78	11.97	9.97	64.27
3.7	14.08+29.95i	5.40+8.17i	15.14	40.68	11.69	9.74	62.42
3.8	13.28+29.16i	5.47+9.25i	15.10	40.67	11.68	9.73	64.61

Load Pull Contours | Efficiency Matched

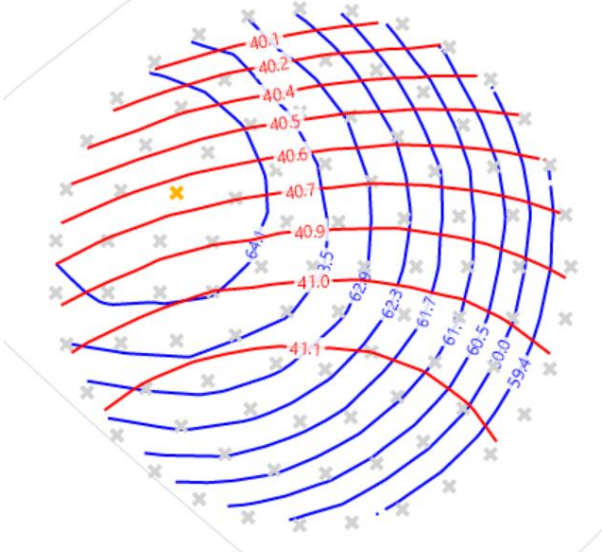
Test conditions, unless otherwise noted: T = +25 °C , V_D = 50V, I_{DQ} = 40mA, Pulse Width = 100usec, Duty Cycle = 5%



[3.6GHz]



[3.7GHz]



[3.8GHz]

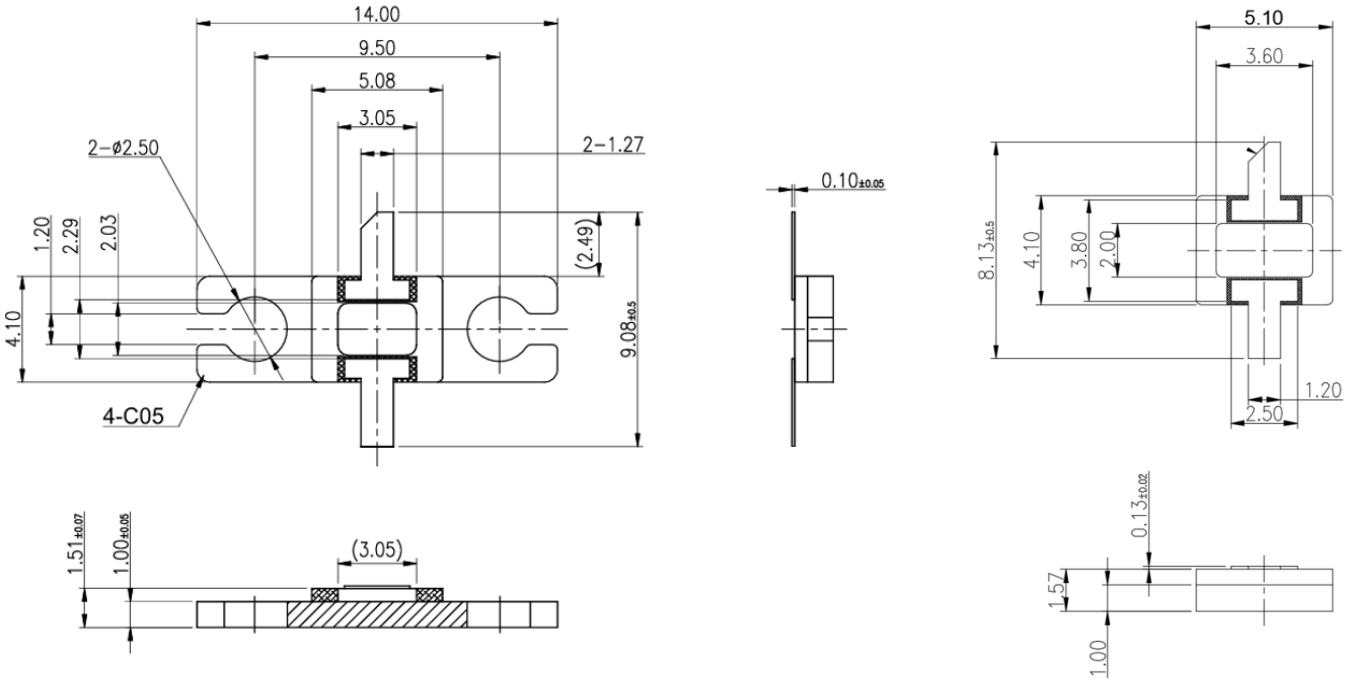
WVP60010F50A

DC – 6.0GHz 10W GaN Amplifier

Package Dimensions

Notes:

1. All dimensions are in millimeters.
2. Dimension tolerance is ± 0.025 mm, unless noted otherwise.





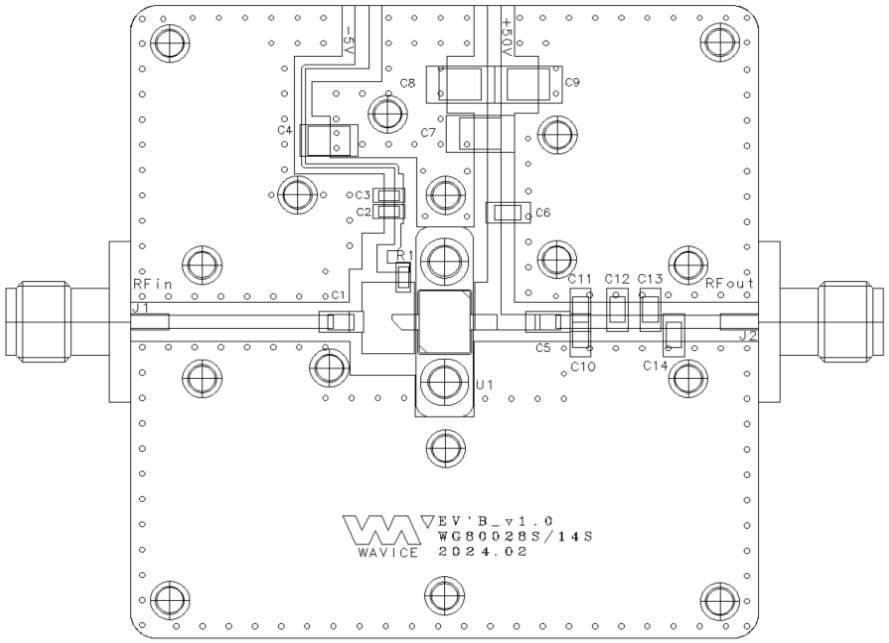
WVP60010F50A

DC – 6.0GHz 10W GaN Amplifier

Evaluation Board

Notes:

1. Evaluation Board Size 50 X 48 [mm]



Bill of Materials

Reference Designator	Value	Description
C1	0.7pF	201 HQ CAP, 200V
C5	2pF	201 HQ CAP, 200V
C6	9.1pF	201 HQ CAP, 200V
C2	10pF	0603 Chip CAP, 50V
C3	1nF	0603 Chip CAP, 50V
C10	0.1pF	201 HQ CAP, 200V
C11, C14	0.2pF	201 HQ CAP, 200V
C12, C13	0.5pF	201 HQ CAP, 200V
C8	10uF	MLCC CAP, 10uF, 100V
R1	5.6 ohm	0603 Chip Res, ±5%
C4, C7, C9	-	NC
U1	10W	Wavice GaN Transistor
PCB Information	RO4350B, 20mil, 1oz	

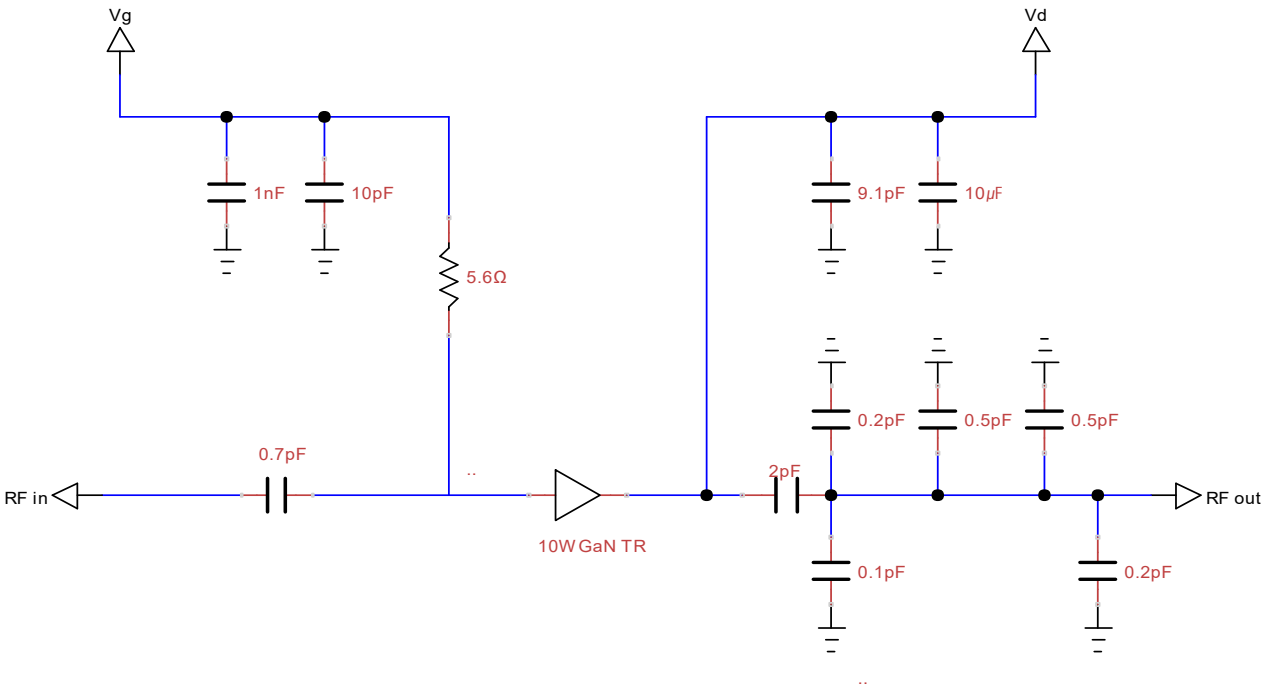
WVP60010F50A

DC – 6.0GHz 10W GaN Amplifier

Applications Information

Notes:

1. Evaluation Board Schematic



Bias-Up & Down Procedure

Procedure	Description
Bias-Up	1. Set I_D limit to 5000 mA, I_G limit to 20 mA
	2. Set V_G to −4.0 V
	3. Set V_D +28V or +50 V
	4. Adjust V_G more positive until I_{DQ}
	5. Apply RF signal
Bias-Down	1. Turn off RF signal
	2. Reduce V_G to −4.0 V. Ensure I_{DQ} ~ 0 mA
	3. Set V_D to 0
	4. Turn off V_D supply
	5. Turn off V_G supply

WVP60010F50A

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Handling Precautions

Parameter	Class	Test Methodology
ESD – Human Body Model (HBM)	Class 1B	JEDEC JESD22 A114-D
ESD – Charged Device Model (CDM)	Class IV	JEDEC JESD22 C101-C
MSL – Moisture Sensitivity Level	N/A	IPC/JEDEC Standard J-STD-020

Solderability

The component leads should be manually soldered, and the package cannot be subjected to conventional reflow processes. The use of no-clean solder to avoid washing after soldering is recommended.

Contact Information

- Web : www.wavice.com
- Tel : +82-31-260-8600
- Email : sales@wavice.com

Notes & Disclaimer

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