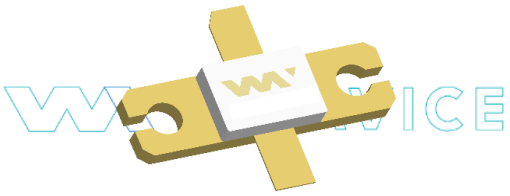
WG80028SF

DC - 8.0GHz 28W GaN Amplifier

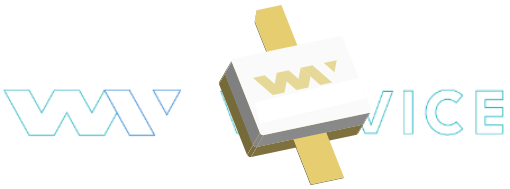
Features

- Frequency Range : DC - 8.0GHz
- Psat : 44.5dBm
- Power Gain : 11.5dB @Psat
- Small Signal Gain : 14dB
- DE : 40% @Psat
- Bias : V_D = 50V, I_{DQ} = 80mA, V_G = -2.5V (Typ.)
- Characterized at Pulse duty 10%, Pulse width 100uS

Product Image



- Package Type : SCF-BC1



- Package Type : SCN-BC1

Description

Wavice's WG80028SF is a high power, C-Band amplifier fabricated on Wavice's Durable 0.3um GaN on SiC process. Covering the frequency range of DC - 8.0GHz, the WG80028SF typically provides 44.5dBm of saturated output power and 11.5dB of power gain while achieving 40% drain efficiency.
The WG80028SF is ideal for use in both commercial and military radar systems.

ROHS compliant.

Applications

- Military Radar
- Commercial Radar
- Infra Structure
- Small Cell

Ordering information

Part No.	Description
WG80028SF	SCF-BC1
WG80028SP	SCN-BC1
WG80028SFEV	Evaluation Board Jig

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Absolute Maximum Ratings

Parameter	Symbol	Value / Range
Drain Source Voltage	V_{DS}	55 V
Gate Source Voltage	V_{GS}	-10 to +2 V
Maximum Forward Gate Current	I_{GMAX}	3.5 mA
Absolute Maximum Channel Temperature	T_{CH}	+250 ℃
Storage Temperature	T_{STG}	-65 ℃ to +150 ℃
Mounting Temperature		245 ℃ / 30 sec

1) Case temperature T_C =25 ℃
2) Wavice does not recommend sustained operation above maximum operating conditions.
3) Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Symbol	Value / Range
Drain Source Voltage	V_{DS}	50V
Drain Current	I_{DQ}	80mA
Gate Source Voltage (Typical)	V_{GS}	-2.5V

1) Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.
2) Proper ESD(electrostatic discharge) control techniques should be used when handling these devices.

Thermal Characteristics

Parameter	Symbol	Units	Value	Test Conditions
Thermal Resistance using Infrared Measurement of Die Surface Temperature	R_{θ}(IR)	℃/W	TBD	Tbase = 85°C, V_D = 50V, I_{DQ} = 80mA, Freq = 3.6GHz - 3.8GHz, P_{diss} = 28W
Peak IR Surface Temperature	T_{CH}	℃	TBD	

1) Thermal resistance determined to the case temperature (85 ℃)
2) Channel temperature indicated is an IR scan equivalent temperature, Thermal resistance is calculated using this value.

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Electrical Specifications

Parameter	Units	Min	Typ	Max
Saturated Output Power [1)]	dBm	44.5		
DE	%	40		
Power Gain	dB	11.5		
Small Signal Gain	dB	14		
Input Return Loss	dB		-5	

Test conditions, unless otherwise noted :

- TA = 25 °C, V_D = 50V, I_{DQ} = 80mA, V_G = -2.5V (Typ.)
- Test Frequency : 3.6GHz - 3.8GHz
- Measured in WG80028SF Evaluation Board

1) Characterized at Pulse duty 10%, Pulse width 100uS

Parameter	Units	Min	Typ	Max	Test Conditions
Gate Threshold Voltage	V	-3.4	-2.7	-2.0	V_{DS}= 10V, I_D= 3.5mA
Drain-Source Breakdown Voltage	V	150			V_{GS}= -8V, I_D= 3.5mA
Drain Current(I_{DMAX})[1)]	A	3.0	3.4		V_{DS}= 10V, V_{GS}= 2.0V
Gate Forward Voltage	V		2		I_{GS}= 3.5mA

Test conditions, unless otherwise noted :

1) Scaled from PCM unit cell

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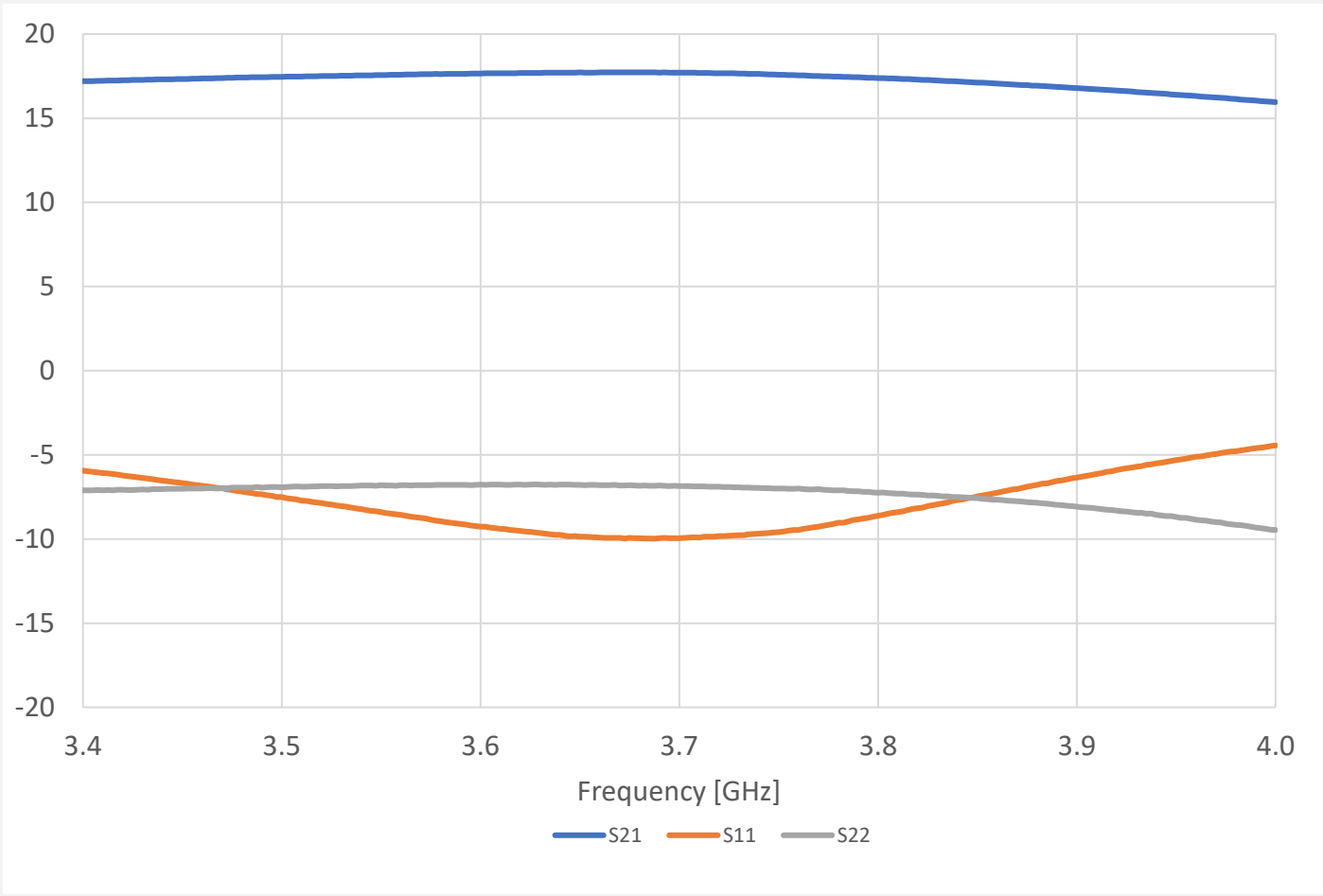
Performance Plots |

Test conditions, unless otherwise noted : T = +25 °C, V_D = 50V, I_{DQ} = 80mA



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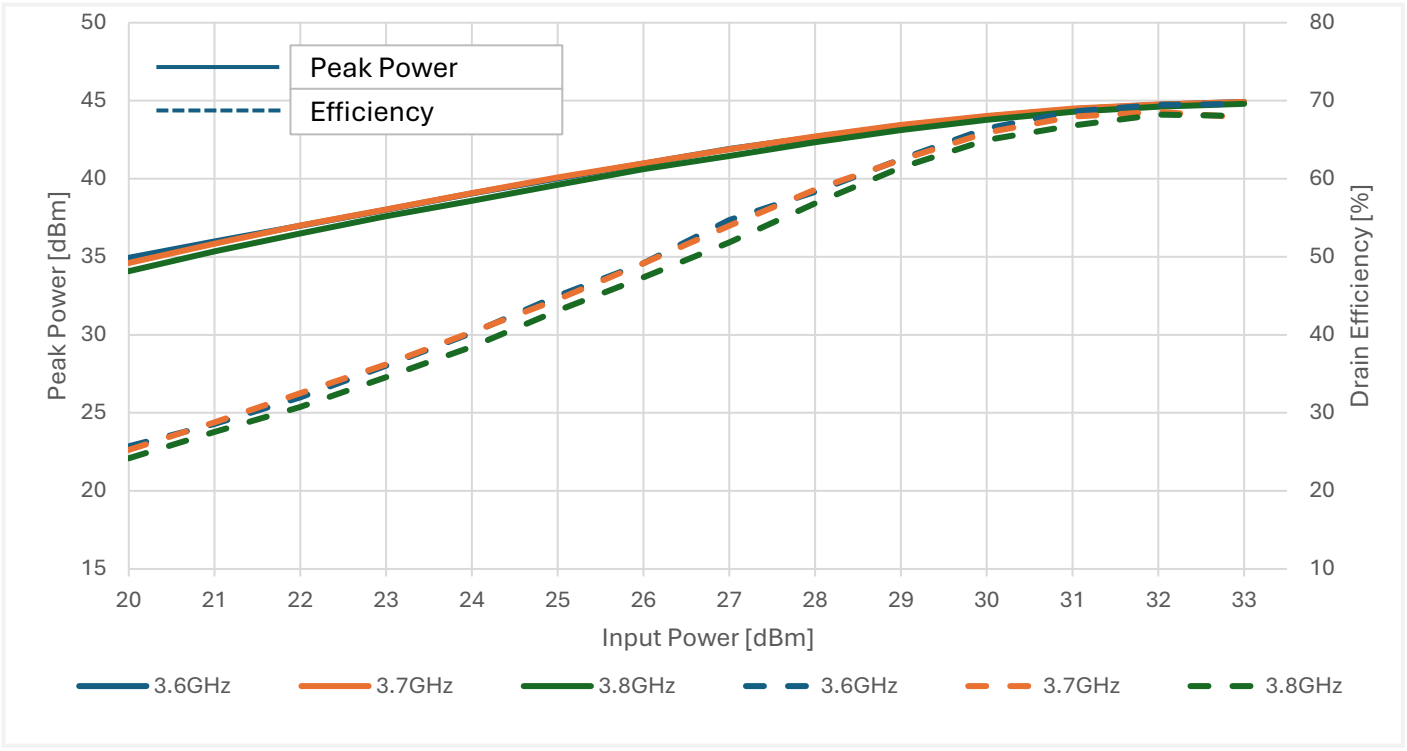
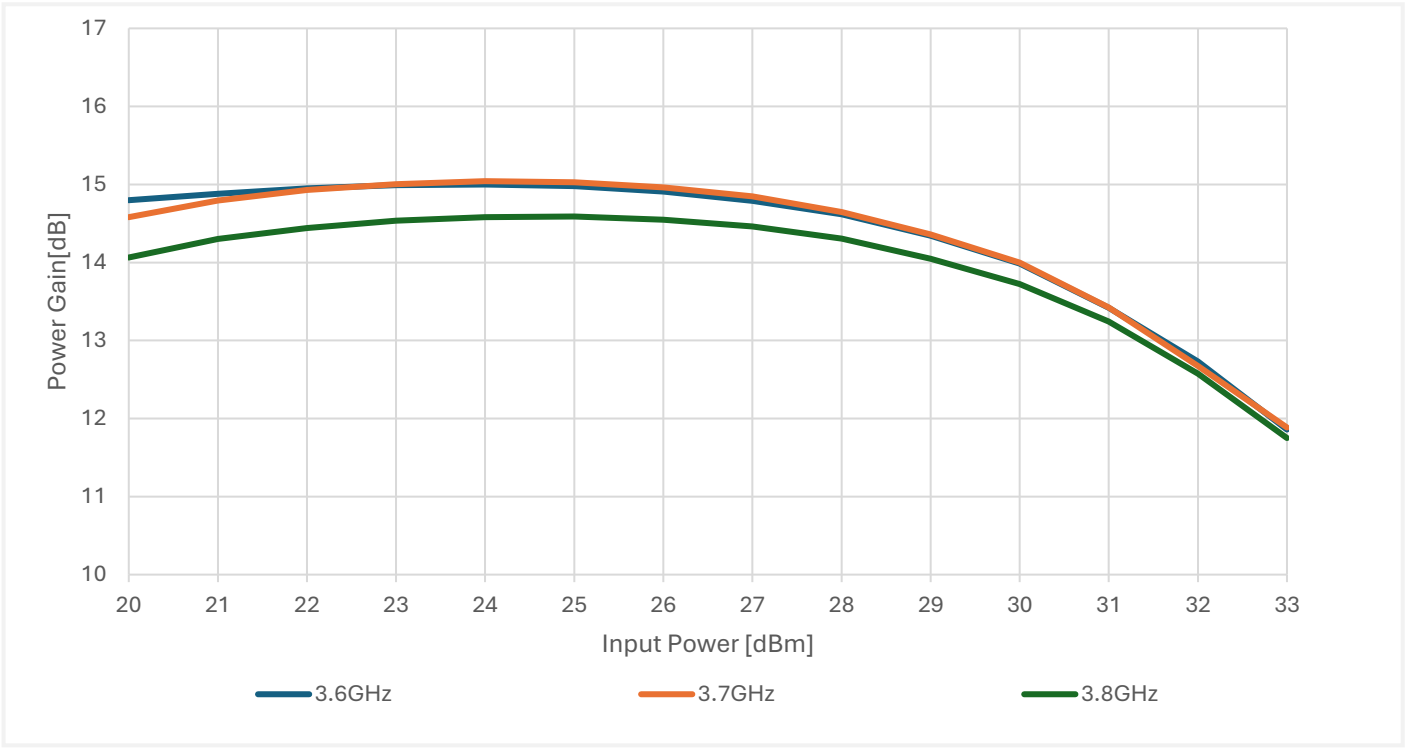
Performance Plots | Peak Power / DE vs Input Power

Test conditions, unless otherwise noted : T = +25 °C, V_D = 50V, I_{DQ} = 80mA, Characterized at Pulse duty 10%, Pulse width 100uS



Performance Plots | Power Gain vs Input Power

Test conditions, unless otherwise noted : T = +25 °C, V_D = 50V, I_{DQ} = 80mA, Characterized at Pulse duty 10%, Pulse width 100uS



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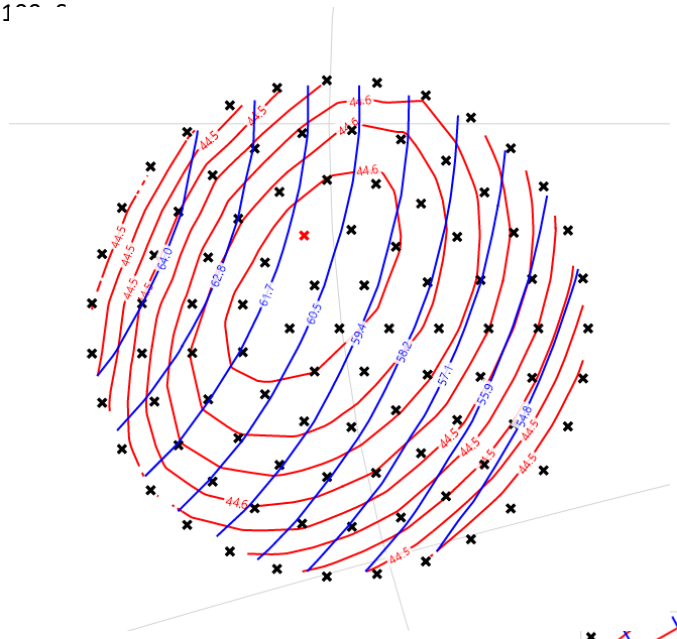
Load Pull Performance Plots | Power Matched

Test conditions, unless otherwise noted : T = +25 °C, V_D = 50V, I_{DQ} = 80mA, Characterized at Pulse duty 10%, Pulse width 100uS

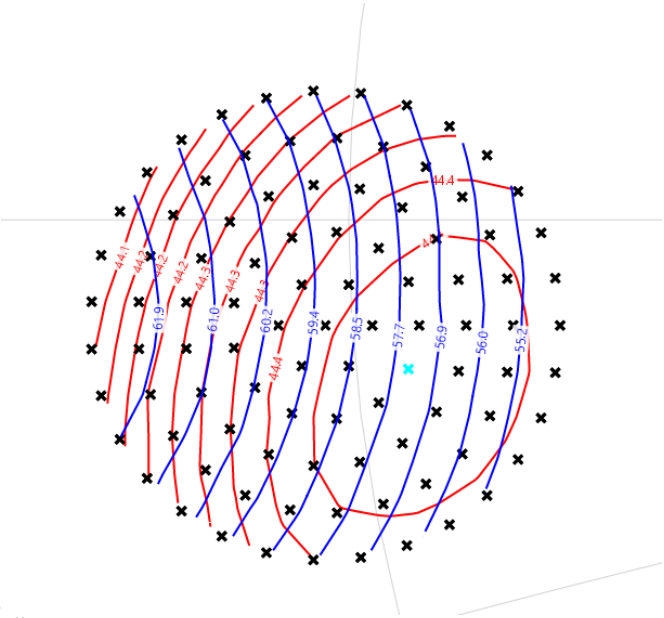
Freq (GHz)	ZL_F0	Zin_F0	Gain (dB)	Pout (dBm)	Pout (W)	Power Density (W/mm)	D.Eff(%)
3.6	24.35-2.48i	4.01+15.32i	13.29	44.64	29.12	11.65	61.31
3.7	26.27-3.70i	3.91+16.46i	13.06	44.45	27.87	11.15	57.41
3.8	27.77-7.14i	4.10+17.61i	12.85	44.43	27.73	11.09	57.24

Load Pull Contours | Power Matched

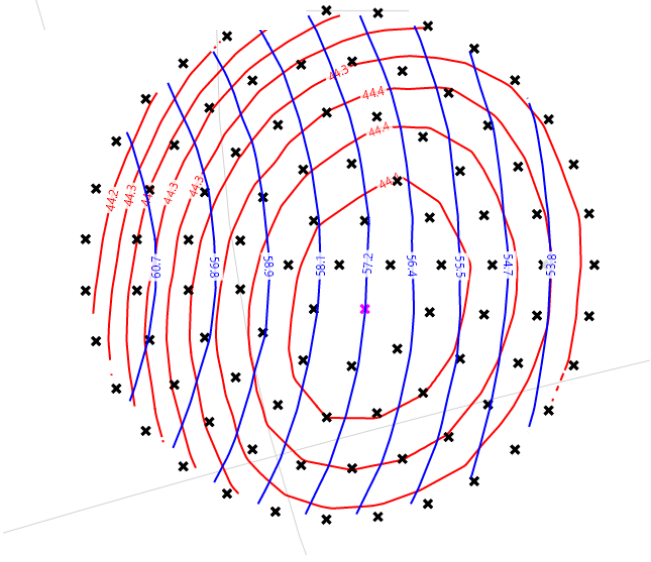
Test conditions, unless otherwise noted : T = +25 °C, V_D = 50V, I_{DQ} = 80mA, Characterized at Pulse duty 10%, Pulse width



[3.6GHz]



[3.7GHz]



[3.8GHz]

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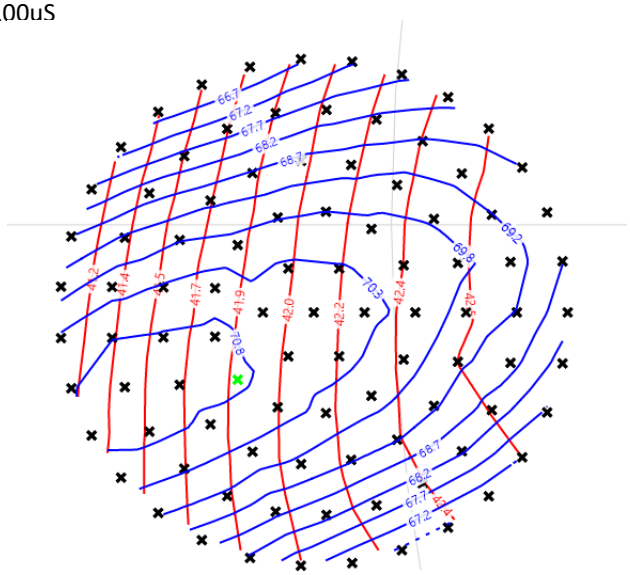
Load Pull Performance Plots | Efficiency Matched

Test conditions, unless otherwise noted : T = +25 °C, V_D = 50V, I_{DQ} = 80mA, Characterized at Pulse duty 10%, Pulse width 100uS

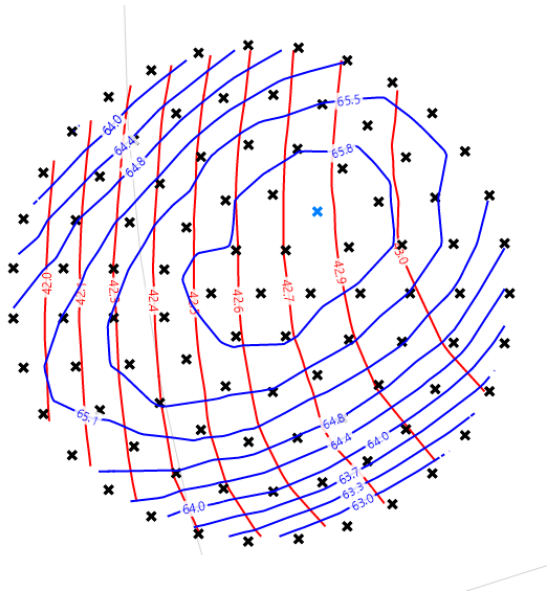
Freq (GHz)	ZL_F0	Zin_F0	Gain (dB)	Pout (dBm)	Pout (W)	Power Density (W/mm)	D.Eff(%)
3.6	6.37-2.03i	2.85+15.03i	15.41	41.43	13.90	5.56	71.28
3.7	12.74-3.42i	3.51+16.15i	15.84	42.83	19.18	7.67	66.21
3.8	13.49-7.00i	3.80+17.13i	15.43	42.77	18.94	7.57	65.98

Load Pull Contours | Efficiency Matched

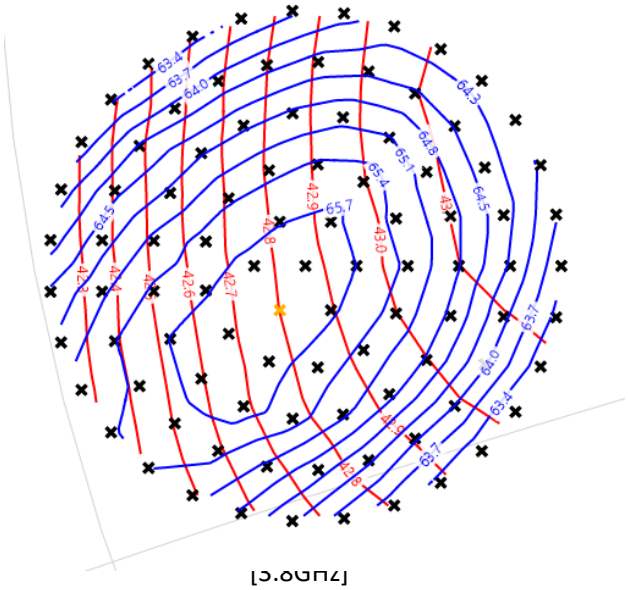
Test conditions, unless otherwise noted : T = +25 °C, V_D = 50V, I_{DQ} = 80mA, Characterized at Pulse duty 10%, Pulse width 100uS



[3.6GHz]



[3.7GHz]



[3.8GHz]

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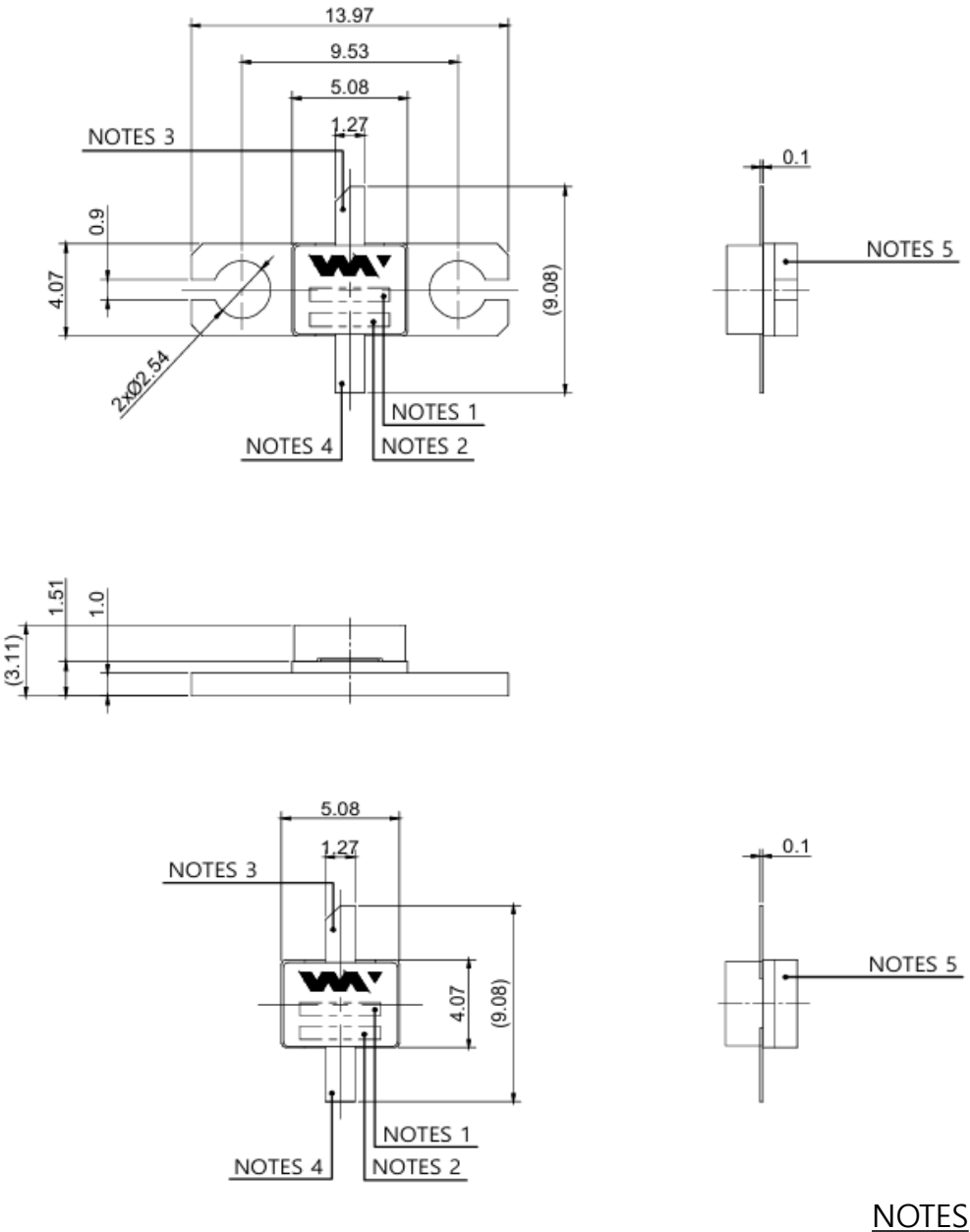
Package Dimensions

Notes:

1. All dimensions are in millimeters.
2. Dimension tolerances are ±0.20 mm for single-decimal dimensions (X.X) and ±0.15 mm for double-decimal dimensions (X.XX), unless otherwise noted..



NOTES

1. Model Name
2. Lot No / Serial No
3. Vg / RF IN
4. Vd / RF out
5. GND

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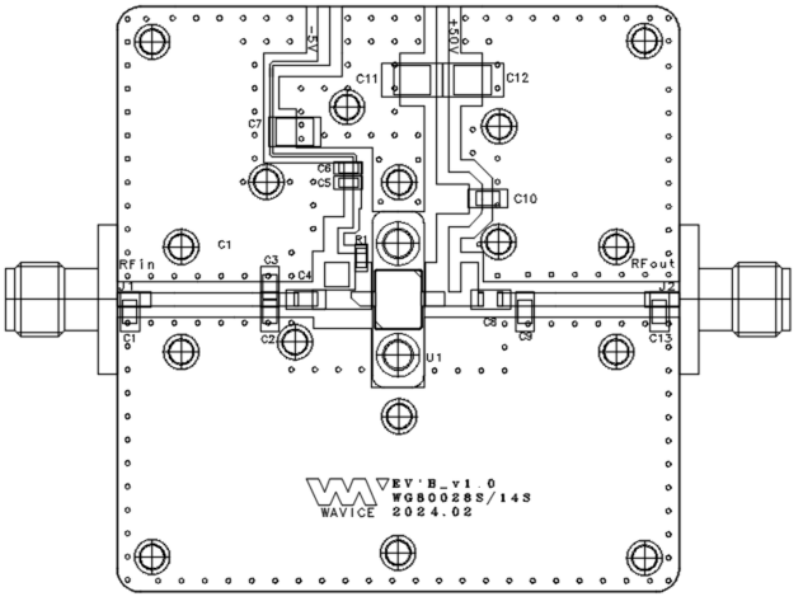
Evaluation Board of 3.6GHz - 3.8GHz

Notes:

1. Evaluation Board Size 48 X 50 [mm]



Bill of Materials

Reference Designator	Value	Description
C1, C3	0.5pF	201 HQ CAP, 200V
C2, C9	0.2pF	201 HQ CAP, 200V
C4, C8	3pF	201 HQ CAP, 200V
C5	10pF	0603 Chip CAP, 50V
C6	1nF	0603 Chip CAP, 50V
C13	0.1pF	201 HQ CAP, 200V
C10	100pF	201 HQ CAP, 200V
C12	10uF	MLCC CAP, 10uF, 100V
R1	5.6 ohm	0603 Chip Res, ±5%
C7, C11	-	NC
U1	28W	WG80055SF
PCB Information	RO4350B, 20mil, 1oz	

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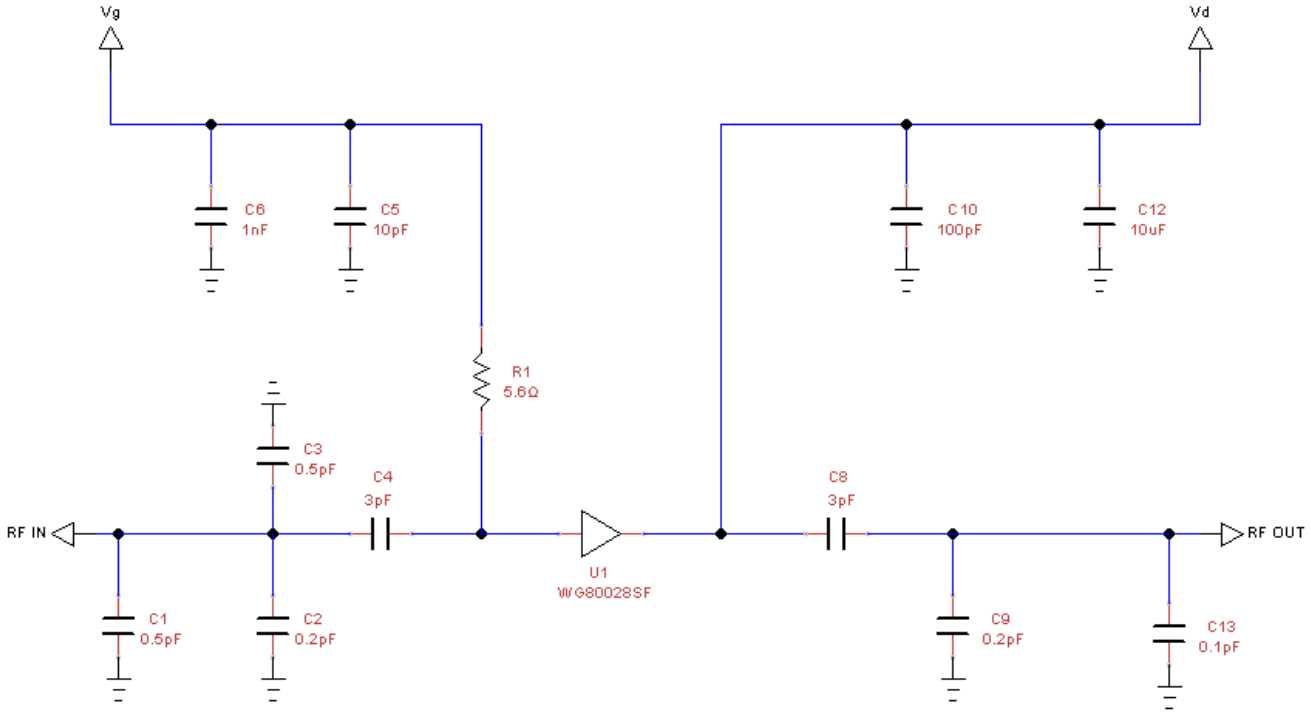
Applications Information

Notes:

1. Evaluation Board Schematic



Bias-Up & Down Procedure

Procedure	Description
Bias-Up	1. Set I_D limit to 5000 mA, IG limit to 20 mA
	2. Set V_G to −4.0 V
	3. Set V_D + 50V
	4. Adjust V_G more positive until I_{DQ}
	5. Apply RF signal

Bias-Down	1. Turn off RF signal
	2. Reduce V_G to −4.0 V. Ensure I_{DQ} ~ 0 mA
	3. Set V_D to 0
	4. Turn off V_D supply
	5. Turn off V_G supply

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Handling Precautions

Parameter	Test Methodology
ESD – Human Body MODEL (HBM)	JEDEC JESD22 A114-D
ESD – Charged Device MODEL (CDM)	JEDEC JESD22 C101-C
MSL – Moisture Sensitivity Level	IPC/JEDEC Standard J-STD-020

Solderability

The component leads should be manually soldered, and the package cannot be subjected to conventional reflow processes. The use of no-clean solder to avoid washing after soldering is recommended.

Contact Information

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- Tel : +82-31-260-8600
- Email : sales@wavice.com

Notes & Disclaimer

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