WG40120SP-LV

2.1 – 2.2GHz 120W GaN Amplifier

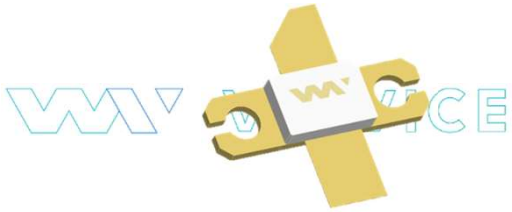
Features

- Frequency Range : 2.1 – 2.2GHz
- Psat : 50.8 dBm
- Power Gain: 8dB
- Small Signal Gain: 10dB
- DE: 55% @Psat
- Bias : V_D = 28V, I_{DQ} = 500mA, V_G = -2.5V (Typ.)
- Characterized at Pulse duty 10%, Pulse width 100uS

Product Image



- Package Type : SCN-BG1



- Package Type : SCF-BG1

Description

Wavice's WG40120SP-LV is a high power, S-Band amplifier fabricated on Wavice's Durable 0.4um GaN on SiC process. Covering the frequency range of 2.1 - 2.2GHz, the WG40120SP-LV typically provides 50.8 dBm of saturated output power and 8 dB of power gain while achieving 55% Drain efficiency.
The WG40120SP-LV is ideal for use in both commercial and military radar systems.

ROHS compliant.

Applications

- Military Radar
- Commercial Radar
- Infra Structure
- Small Cell

Ordering information

Part No.	Description
WG40120SF-LV	SCF-BG1
WG40120SP-LV	SCN-BG1
WG40120SF-LVEV	WG40120SF-LV Evaluation Board
WG40120SP-LVEV	WG40120SP-LV Evaluation Board

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Absolute Maximum Ratings

Parameter	Symbol	Value / Range
Drain Source Voltage	V_{DS}	55 V
Gate Source Voltage	V_{GS}	-10 to +2 V
Maximum Forward Gate Current	I_{GMAX}	44 mA
Absolute Maximum Channel Temperature	T_{CH}	+250 ℃
Storage Temperature	T_{STG}	-65 ℃ to +150 ℃
Mounting Temperature		245 ℃ / 30 sec

1) Case temperature T_C =25 ℃
2) Wavice does not recommend sustained operation above maximum operating conditions.
3) Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Symbol	Value / Range
Drain Source Voltage	V_{DS}	28 V
Drain Current	I_{DQ}	500 mA
Gate Source Voltage (Typical)	V_{GS}	-2.5 V
Case Operating Temperature		~40 ℃ to +85 ℃

1) Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.
2) Proper ESD(electrostatic discharge) control techniques should be used when handling these devices.

Thermal Characteristics

Parameter	Symbol	Units	Value	Test Conditions
Thermal Resistance using Infrared Measurement of Die Surface Temperature	R_{θ}(IR)	℃/W	TBD	Tbase = 85°C, V_D = 28V, I_{DQ} = 500mA, Freq = 2.1-2.2GHz
Peak IR Surface Temperature	T_{CH}	℃	TBD	

1) Thermal resistance determined to the case temperature (85 ℃)
2) Channel temperature indicated is an IR scan equivalent temperature, Thermal resistance is calculated using this value.

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Electrical Specifications

Parameter	Units	Min	Typ	Max
Saturated Output Power [1)]	dBm		50.8	
Drain Efficiency	%		55	
Power Gain	dB		8	
Small Signal Gain	dB		10	
Input Return Loss	dB		-5	

Test conditions, unless otherwise noted :

- T_A = 25 °C, V_D = 28V, I_{DQ} = 500mA, V_G = -2.5V (Typ.)
- Test Frequency : 2.1-2.2GHz
- Measured in WG40120SP-LV Evaluation Board

1) Characterized at Pulse duty 10%, Pulse width 100uS

Parameter	Units	Min	Typ	Max	Test Conditions
Gate Threshold Voltage	V	-3.8	-2.7	-2.0	V_{DS}= 10V, I_D= 44 mA
Drain-Source Breakdown Voltage	V	150			V_{GS}= -8V, I_D= 44 mA
Drain Current(I_{DMAX})[1)]	A	33.0	41.8		V_{DS}= 10V, V_{GS}= 2.0V
Gate Forward Voltage	V		2		I_{GS}= 44 mA

Test conditions, unless otherwise noted :

1) Scaled from PCM unit cell

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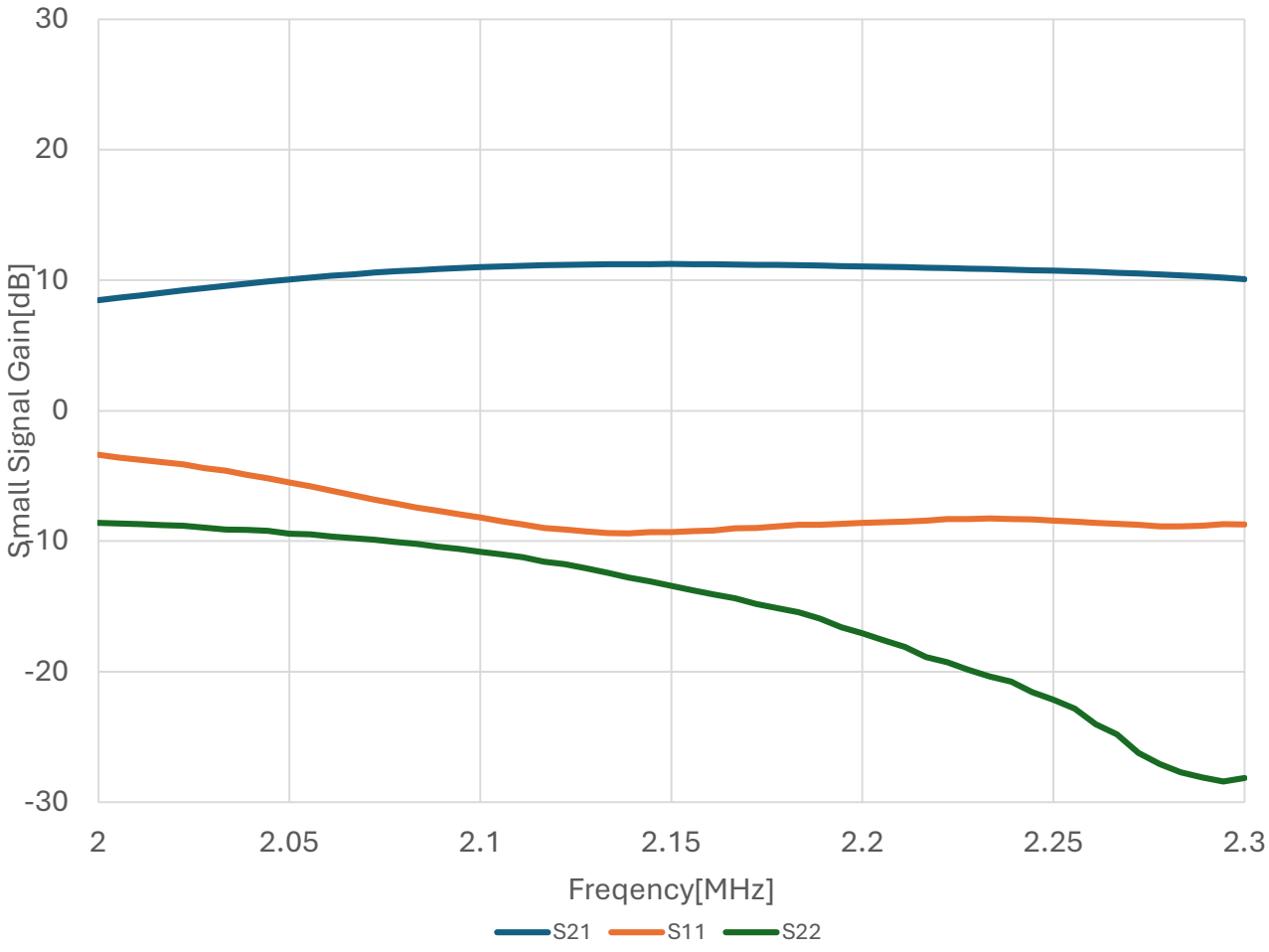
Performance Plots | S-Parameter

Test conditions, unless otherwise noted: T = +25 °C, V_D = 28V, I_{DQ} = 500mA



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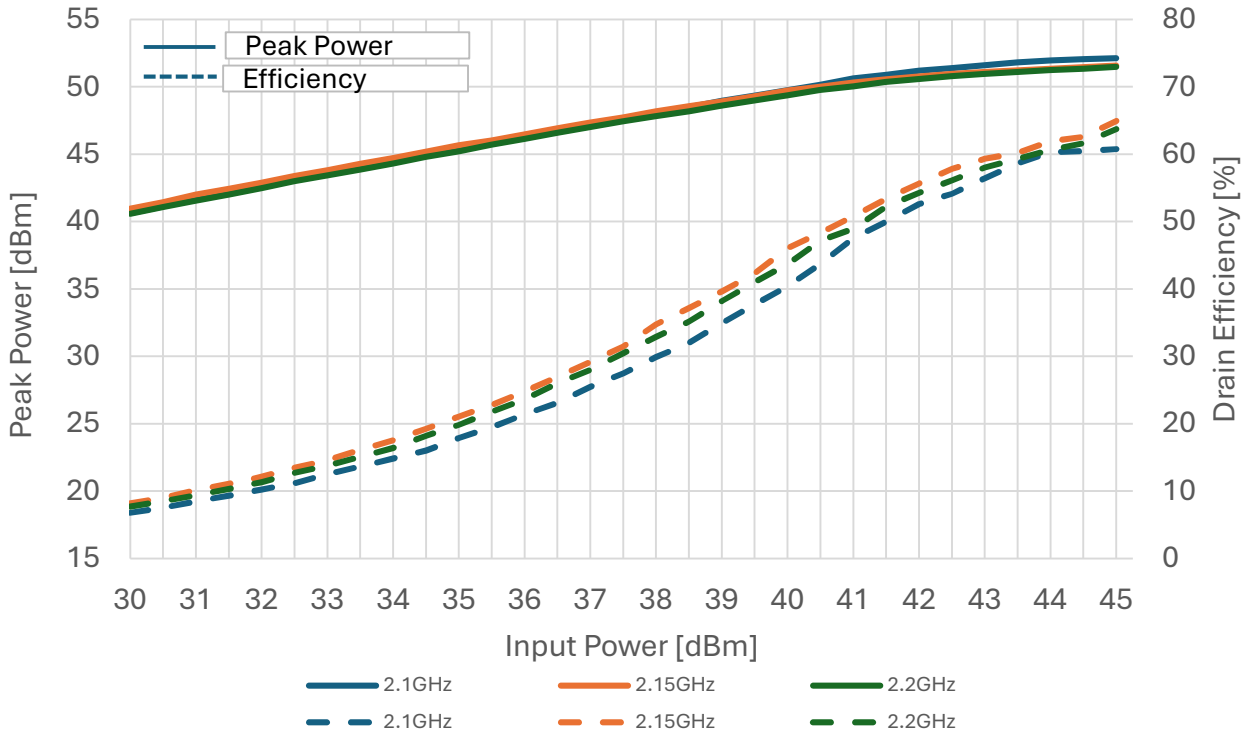
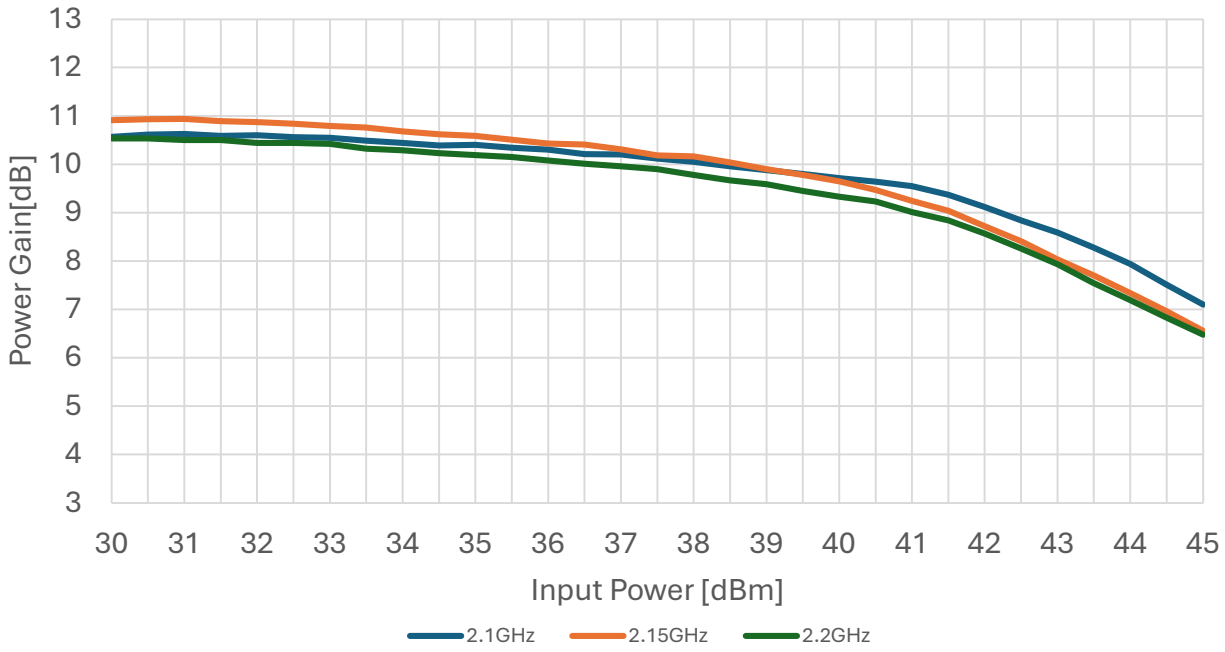
Performance Plots | Peak Power / DE vs Input Power

Test conditions, unless otherwise noted: T = +25 °C, V_D = 28 V, Pulse duty 10%, Pulse width 100uS



Performance Plots | Power Gain vs Input Power

Test conditions, unless otherwise noted: T = +25 °C, V_D = 28 V, Pulse duty 10%, Pulse width 100uS



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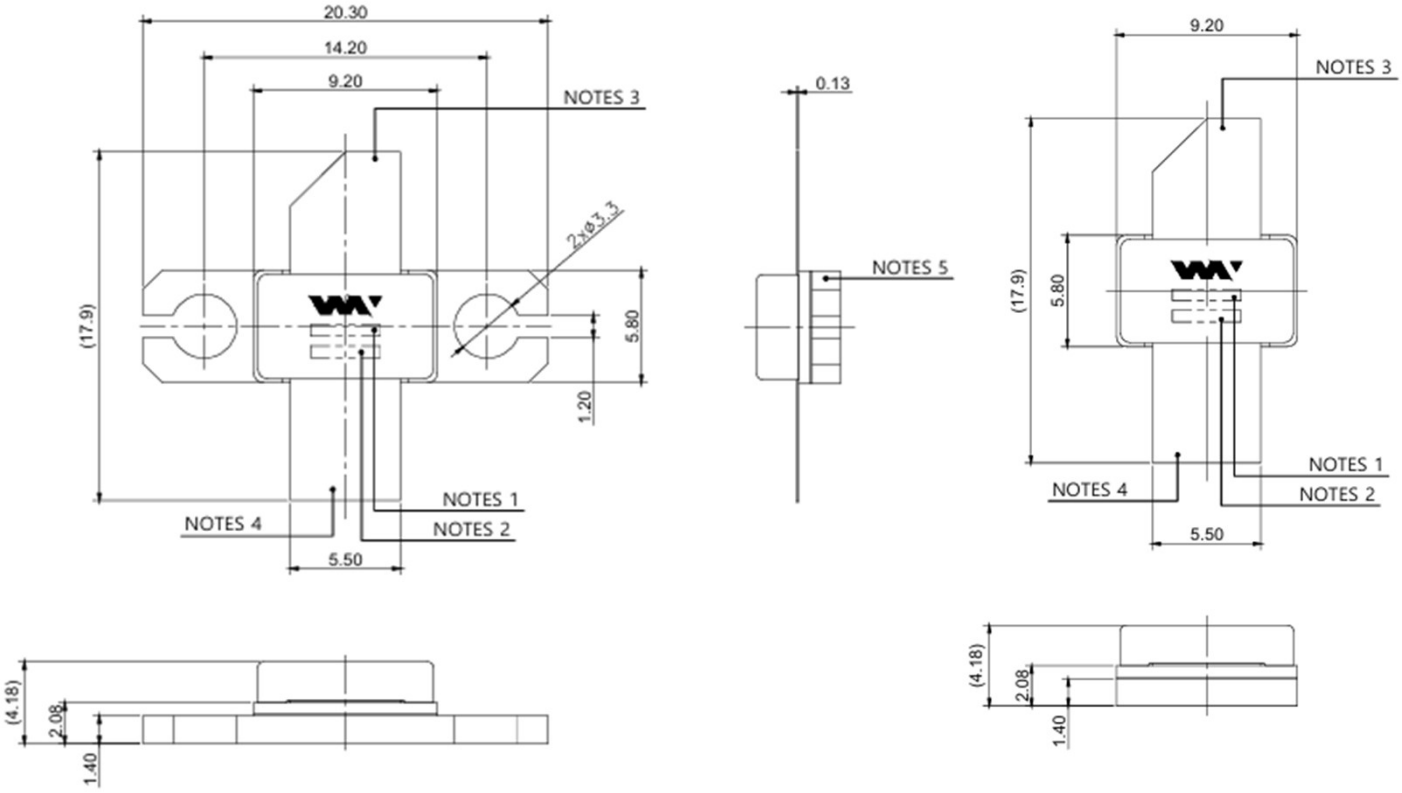
Package Dimensions

Notes:
1. All dimensions are in millimeters.
2. Dimension tolerances are ±0.20 mm for single-decimal dimensions (X.X) and ±0.15 mm for double-decimal dimensions (X.XX), unless otherwise noted.



NOTES
1. Model Name
2. Lot No / Serial No
3. Vg / RF IN
4. Vd / RF out
5. GND

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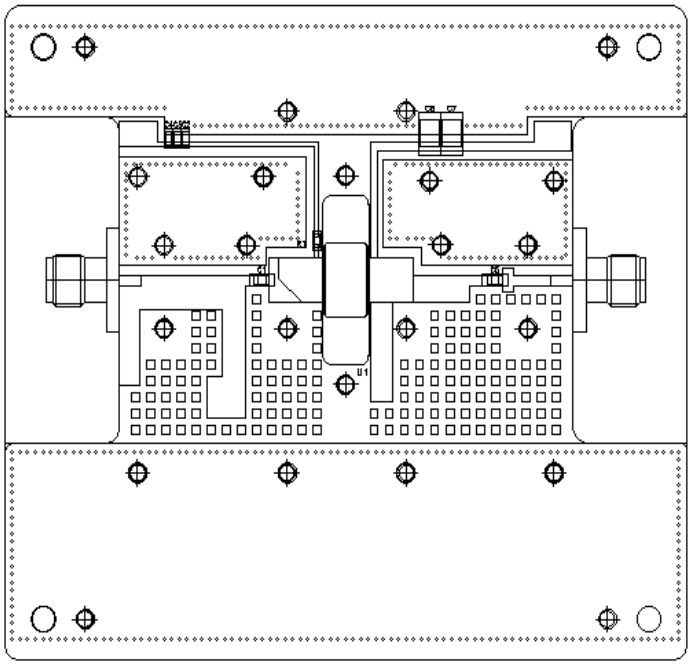
Evaluation Board

Notes:

1. Evaluation Board Size 90 X 80 [mm]



Bill of Materials

Reference Designator	Value	Description
C1	2pF	201 HQ CAP, 200V
C2	100pF	0603 Chip CAP, 50V
C3	1nF	0603 Chip CAP, 50V
C4	10uF	0603 Chip CAP, 50V
C5	2pF	201 HQ CAP, 200V
C6	10uF	MLCC CAP, 10uF, 100V
C7	10uF	MLCC CAP, 10uF, 100V
R1	10Ω	0603 Chip Res, ±5%
U1	120W	WG40120SP-LV
PCB Information	RO4350B, 20mil, 1oz	

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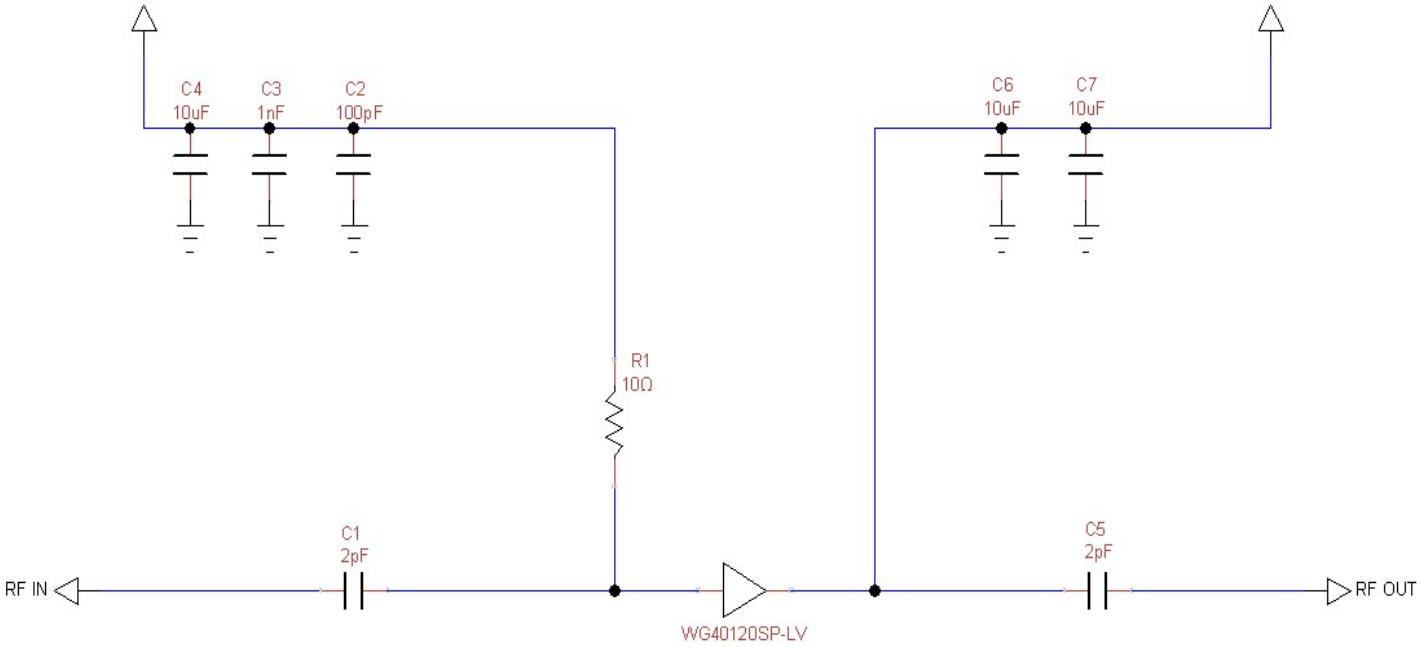
Applications Information

Notes:

1. Evaluation Board Schematic



Bias-Up & Down Procedure

Procedure	Description
Bias-Up	1. Set I_D limit to 5000 mA, I_G limit to 20 mA
	2. Set V_G to −4.0 V
	3. Set V_D +28 V
	4. Adjust V_G more positive until I_{DQ}
	5. Apply RF signal
Bias-Down	1. Turn off RF signal
	2. Reduce V_G to −4.0 V. Ensure I_{DQ} ~ 0 mA
	3. Set V_D to 0
	4. Turn off V_D supply
	5. Turn off V_G supply

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Handling Precautions

Parameter	Class	Test Methodology
ESD – Human Body Model (HBM)	Class 1B	JEDEC JESD22 A114-D
ESD – Charged Device Model (CDM)	Class IV	JEDEC JESD22 C101-C
MSL – Moisture Sensitivity Level	N/A	IPC/JEDEC Standard J-STD-020

Solderability

The component leads should be manually soldered, and the package cannot be subjected to conventional reflow processes. The use of no-clean solder to avoid washing after soldering is recommended.

Contact Information

- Web : www.wavice.com
- Tel : +82-31-260-8600
- Email : sales@wavice.com

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