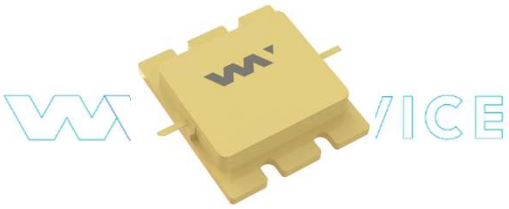
WVI2933250F48

2.9 – 3.3 GHz 250W GaN Amplifier

Features

- Frequency Range : 2.9 – 3.3 GHz
- Psat : 54 dBm
- Power Gain : 13 dB @ Psat
- Small Signal Gain: 16 dB (Typ.)
- PAE: 53% @ Psat
- Bias : V_D = 48V, I_{DQ} = 20mA, V_G = -2.5V (Typ.)
- Characterized at Pulse duty 20%, Pulse width 1000us

Product Image



- Package Type : SKF-QO1

Description

Wavice's WVI2933250F48 is a high power, S-Band amplifier fabricated on Wavice's Durable 0.3um GaN on SiC process. Covering the frequency range of 2.9 – 3.3 GHz, the WVI2933250F48 typically provides 54 dBm of saturated output power and 13 dB of power gain while achieving 53% Power Added efficiency.
The WVI2933250F48 is ideal for use in both commercial and military radar systems.

ROHS compliant.

Applications

- Military Radar
- Commercial Radar
- Infra Structure
- Small Cell

Ordering information

Part No.	Description
WVI2933250F48	SKF-QO1
WVI2933250F48EV	WVI2933250F48 Evaluation Board

WVI2933250F48

2.9 – 3.3GHz 250W GaN Amplifier

Absolute Maximum Ratings

Parameter	Symbol	Value / Range
Drain Source Voltage	V_{DS}	55 V
Gate Source Voltage	V_{GS}	-10 to +2 V
Maximum Forward Gate Current	I_{GMAX}	32 mA
Absolute Maximum Channel Temperature	T_{CH}	+250 ℃
Storage Temperature	T_{STG}	-65 ℃ to +150 ℃
Mounting Temperature		245 ℃ / 30 sec

1) Case temperature T_C =25 ℃
2) Wavice does not recommend sustained operation above maximum operating conditions.
3) Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Symbol	Value / Range
Drain Source Voltage	V_{DS}	48 V
Drain Current	I_{DQ}	20 mA
Gate Source Voltage (Typical)	V_{GS}	-2.5 V
Case Operating Temperature		~40 ℃ to +85 ℃

1) Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.
2) Proper ESD(electrostatic discharge) control techniques should be used when handling these devices.

Thermal Characteristics

Parameter	Symbol	Units	Value	Test Conditions
Thermal Resistance using Infrared Measurement of Die Surface Temperature	R_{θ}(IR)	℃/W	0.33	Tbase = 85°C, V_D = 48V, I_{DQ} = 20mA, Freq = 2.9 ─ 3.3 GHz
Peak IR Surface Temperature	T_{CH}	℃	116.4	

1) Thermal resistance determined to the case temperature (85 ℃)
2) Channel temperature indicated is an IR scan equivalent temperature, Thermal resistance is calculated using this value.

WVI2933250F48

2.9 – 3.3GHz 250W GaN Amplifier

Electrical Specifications

Parameter	Units	Min	Typ	Max
Saturated Output Power [1)]	dBm	54		
PAE @ Psat	%	53		
Power Gain @ Psat	dB	13		
Small Signal Gain	dB		16	
Input Return Loss	dB		-5	
Output Return Loss	dB		-9	

Test conditions, unless otherwise noted :

- TA = 25 °C, V_D = 48V, I_{DQ} = 20mA, V_G = -2.5V(Typ.)
- Test Frequency : 2.9 – 3.3GHz
- Measured in WVI2933250F48 Evaluation Board

1) Pulse width 1000usec, Pulse Duty 20%

Parameter	Units	Min	Typ	Max	Test Conditions
Gate Threshold Voltage	V	-3.8	-2.7	-2.0	V_{DS}= 10V, I_D= 42.0 mA
Drain-Source Breakdown Voltage	V	150			V_{GS}= -8V, I_D= 42.0 mA
Drain Current(I_{DMAX})[1)]	A	35.7	40.3		V_{DS}= 10V, V_{GS}= 2.0V
Gate Forward Voltage	V		2		I_{GS}= 42.0 mA

Test conditions, unless otherwise noted :

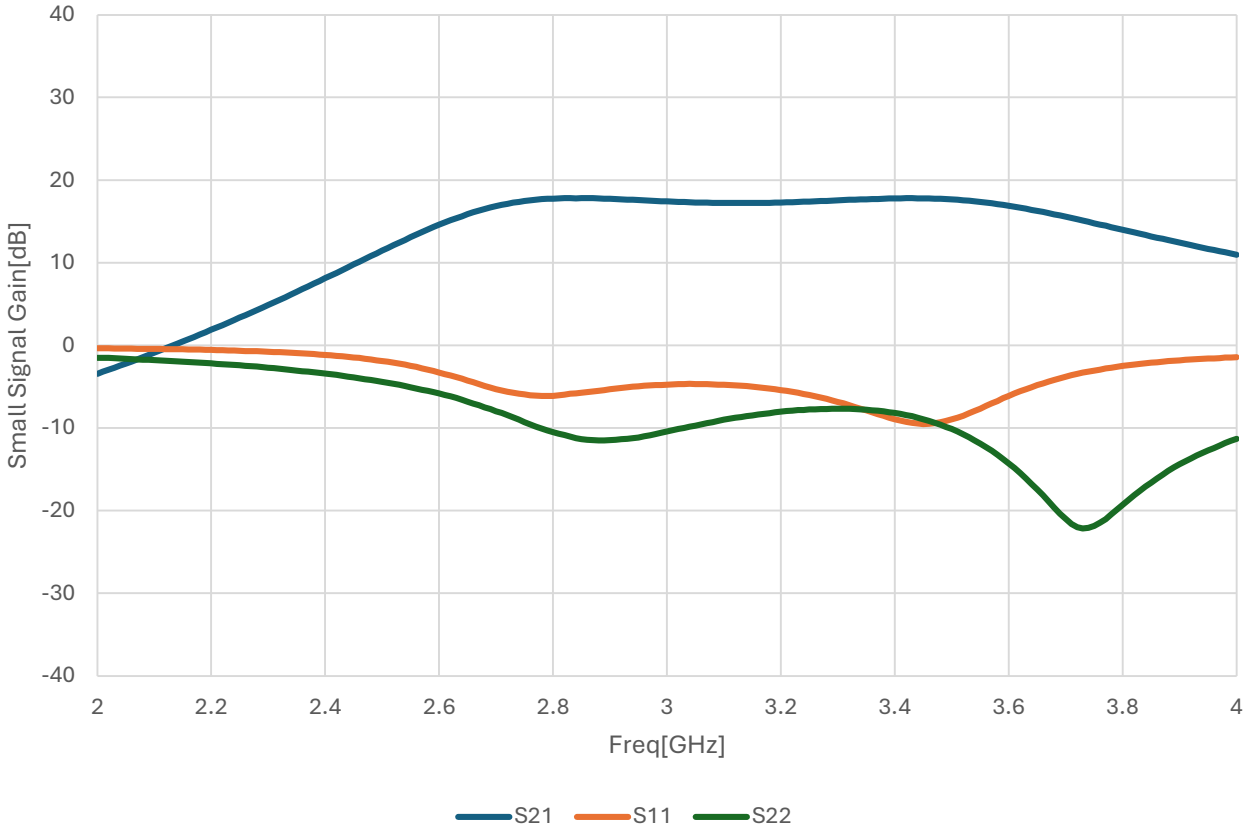
1) Scaled from PCM unit cell

WVI2933250F48

2.9 – 3.3GHz 250W GaN Amplifier

Performance Plots | S-Parameter

Test conditions, unless otherwise noted: T = +25 °C, V_D = 48 V, I_{DQ} = 800 mA

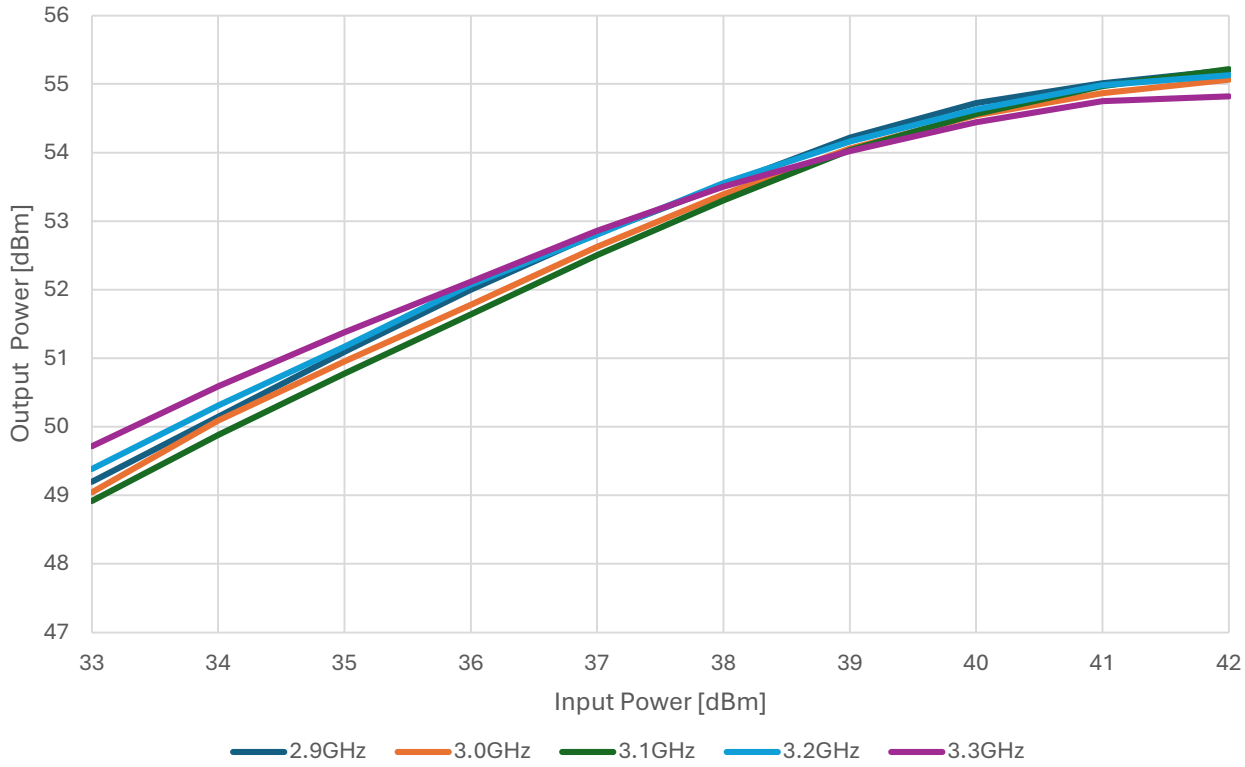


WVI2933250F48

2.9 – 3.3GHz 250W GaN Amplifier

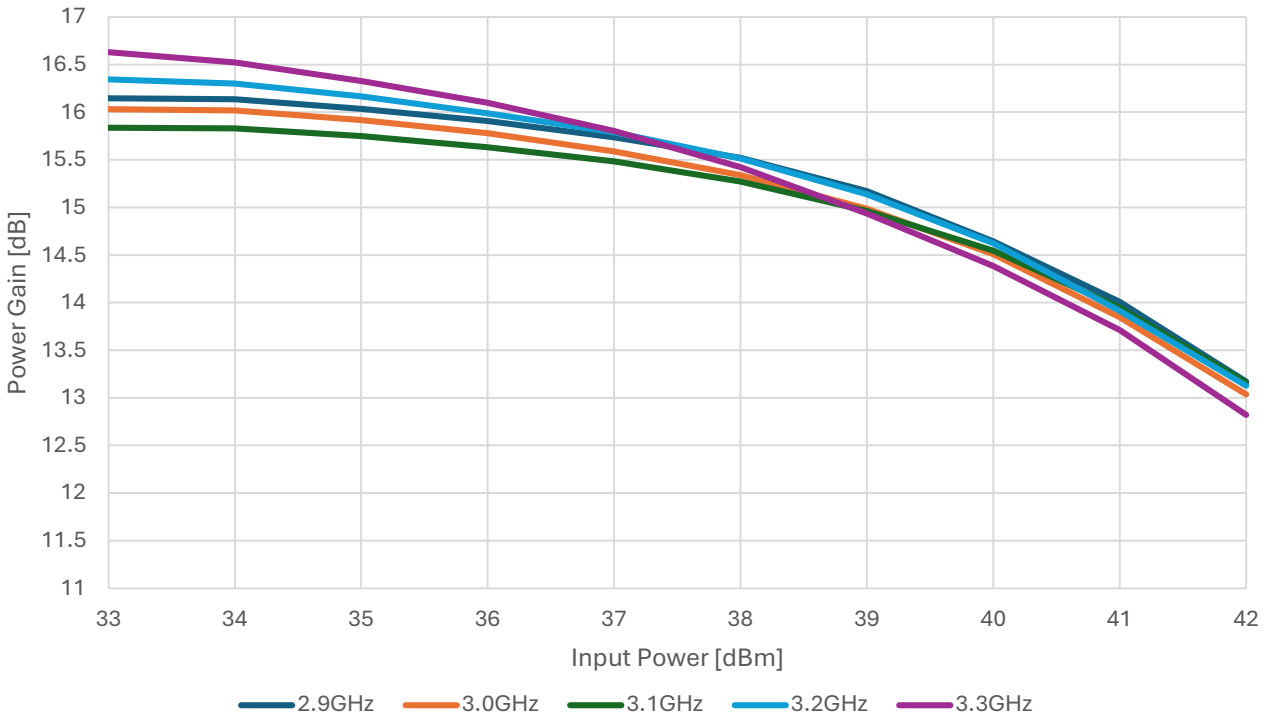
Performance Plots | Output Power vs Input Power

Test conditions, unless otherwise noted: T = +25 °C, V_D = 48 V, I_{DQ} = 20 mA, Pulse Width =1000usec, Duty Cycle = 20%



Performance Plots | Power Gain vs Input Power

Test conditions, unless otherwise noted: T = +25 °C, V_D = 48 V, I_{DQ} = 20 mA, Pulse Width =1000usec, Duty Cycle = 20%

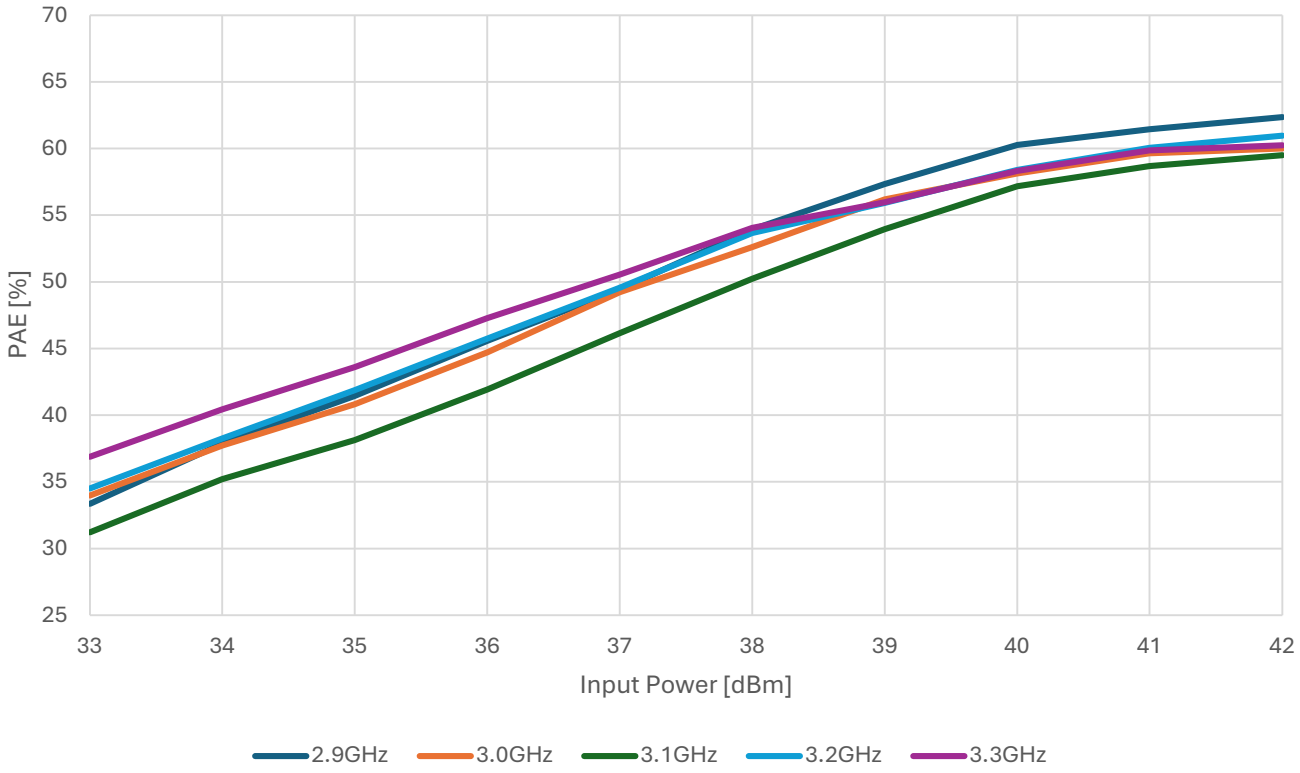


WVI2933250F48

2.9 – 3.3GHz 250W GaN Amplifier

Performance Plots | PAE vs Input Power

Test conditions, unless otherwise noted: T = +25 °C, V_D = 48 V, I_{DQ} = 20 mA, Pulse Width =1000usec, Duty Cycle = 20%



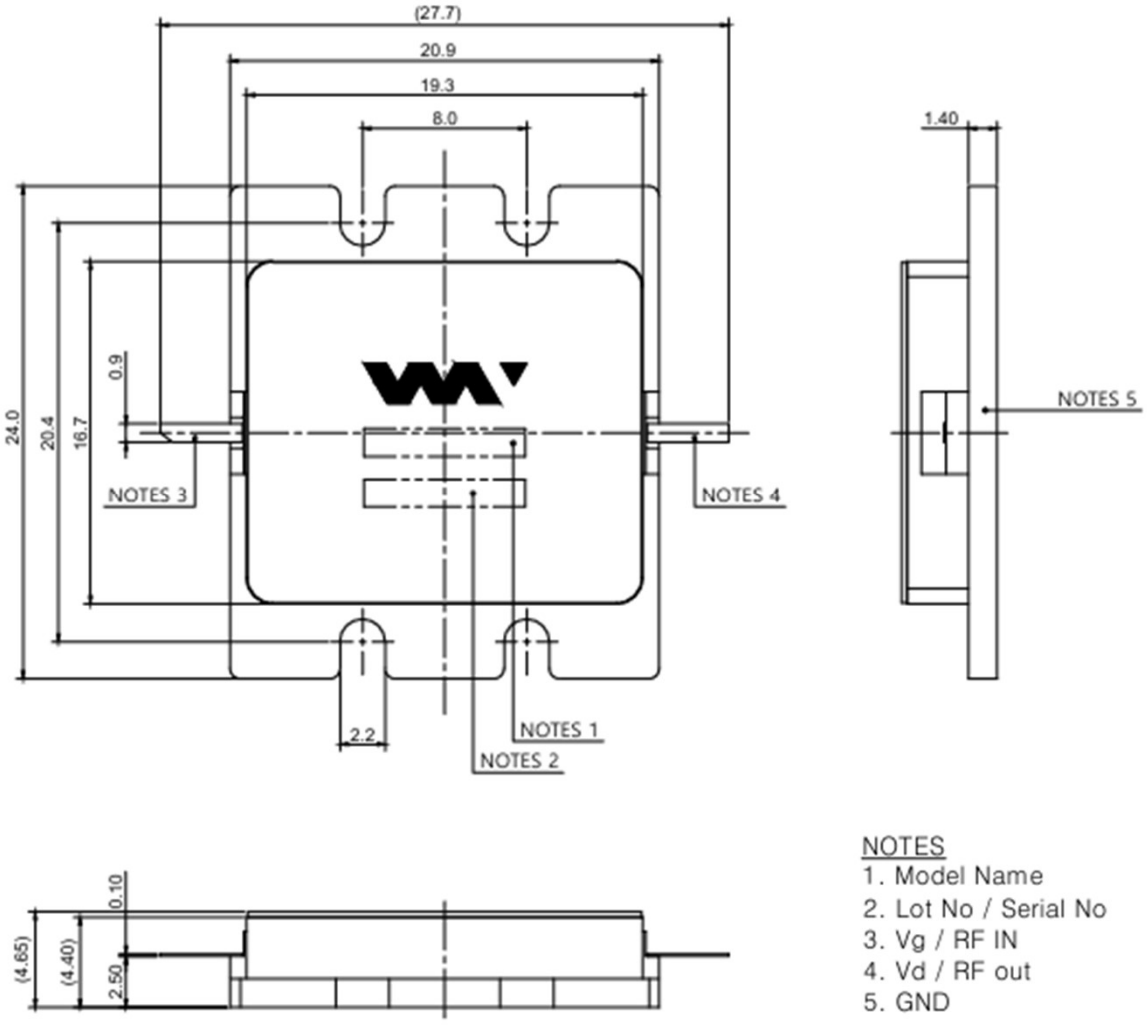
WVI2933250F48

2.9 – 3.3GHz 250W GaN Amplifier

Package Dimensions

Notes:

1. All dimensions are in millimeters.
2. Dimension tolerances are ±0.20 mm for single-decimal dimensions (X.X) and ±0.15 mm for double-decimal dimensions (X.XX), unless otherwise noted.



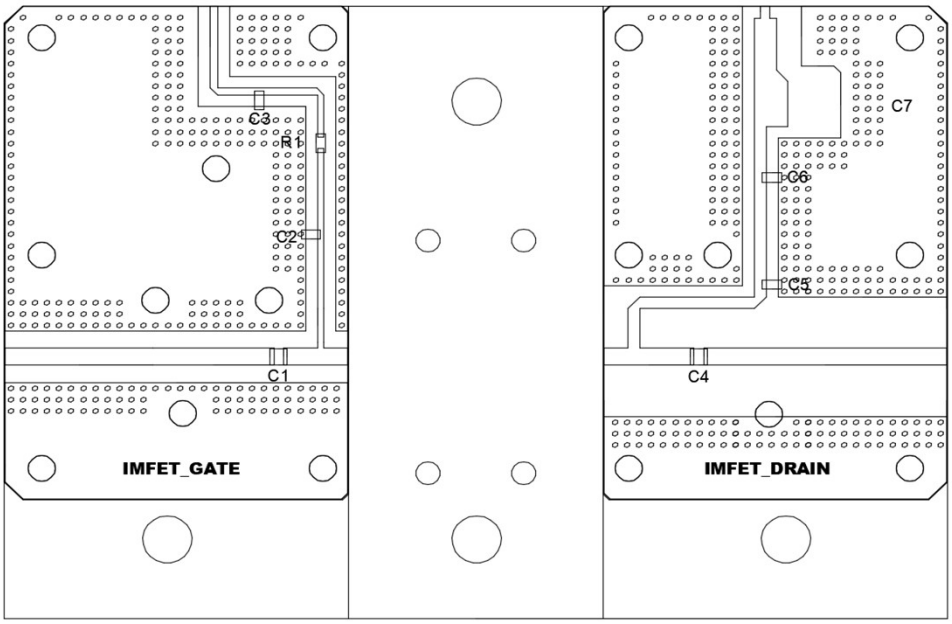
WVI2933250F48

2.9 – 3.3GHz 250W GaN Amplifier

Evaluation Board

Notes:

1. Evaluation Board Size 53.7 X 78.2 [mm]



Bill of Materials

Reference Designator	Value	Description
C1	0.7pF	800A0R7B250XT
C2	10pF	GRM1885C2A100JA01D
C3	470pF	GRM1885C2A471JA01D
C4	4.7pF	800A4R7BT250XT
C5	10pF	800A100JT250XT
C6	100pF	800A101JT250XT
C7	220uF	EEE-FK2A221AM
R1	51ohm	CR-03JL7---51R
U1		WVI2933250F48
PCB Information	TLY-3, 20Mil, 1oz	

WVI2933250F48

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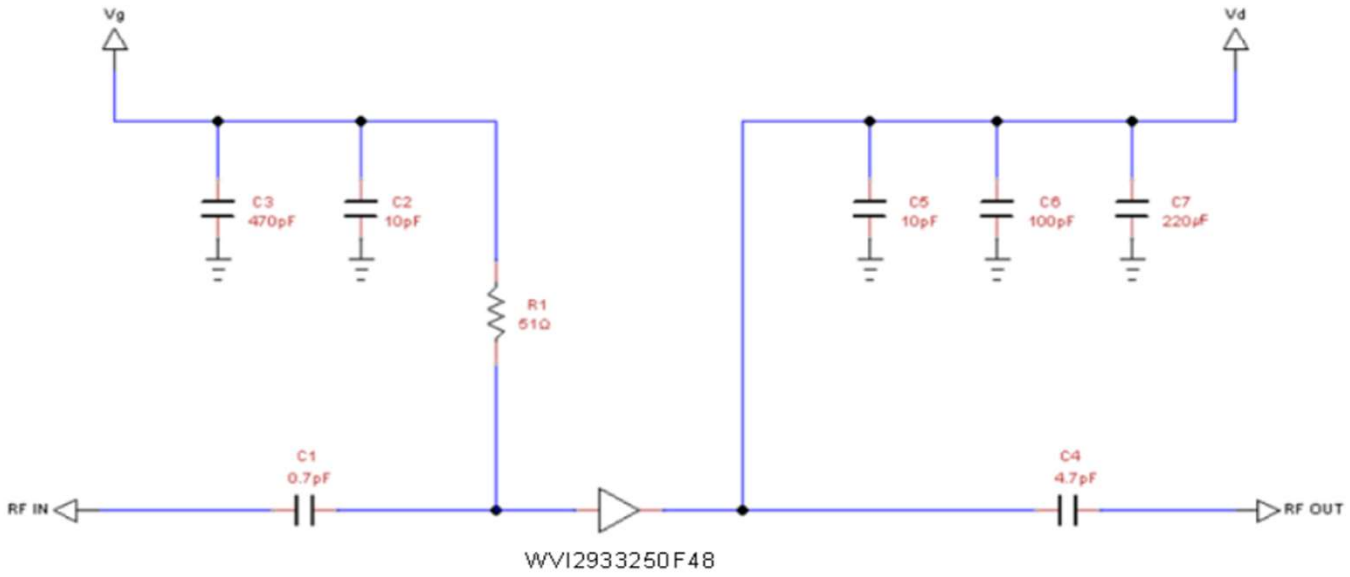
Applications Information

Notes:

1. Evaluation Board Schematic



Bias-Up & Down Procedure

Procedure	Description
Bias-Up	1. Set I_D limit to 5000 mA, I_G limit to 20 mA
	2. Set V_G to −4.0 V
	3. Set V_D +48 V
	4. Adjust V_G more positive until I_{DQ}
	5. Apply RF signal
Bias-Down	1. Turn off RF signal
	2. Reduce V_G to −4.0 V. Ensure I_{DQ} ~ 0 mA
	3. Set V_D to 0
	4. Turn off V_D supply
	5. Turn off V_G supply

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Handling Precautions

Parameter	Class	Test Methodology
ESD – Human Body Model (HBM)	Class 1B	JEDEC JESD22 A114-D
ESD – Charged Device Model (CDM)	Class IV	JEDEC JESD22 C101-C
MSL – Moisture Sensitivity Level	N/A	IPC/JEDEC Standard J-STD-020

Solderability

The component leads should be manually soldered, and the package cannot be subjected to conventional reflow processes. The use of no-clean solder to avoid washing after soldering is recommended.

Contact Information

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Notes & Disclaimer

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